Integrated Circuit Implementation for a GaN HFETs Driver Circuit

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***Abstract*- The paper presents the design of an integrated circuit (IC) for a 10MHz low power-loss driver for GaN HFETs. While the main elements of the topology were introduced in a previous work, here the authors focus on the design of the IC and present preliminary results and considerations.**

The driver circuit proposed, based upon new two-stage positive-to-negative level shifters and resonant topology, has been designed and implemented using the cost-effective Smart Voltage eXtension (SVX) technique. Detailed analysis of the design process as well as a full set of simulations, reported in the paper, fully demonstrate the possibility to exploit the advantages of GaN devices by means of a smart and convenient implementation.

I. INTRODUCTION

The rapidly developing research on wide-band III-Nitride semiconductor materials (such as GaN) has been driven by the unique properties of these materials, making the III-Nitride technology a promising approach for high-power, high-temperature applications[1][2][3]. These devices can be extremely useful in industrial power electronic applications and can improve the efficiency and the regulation in AC-DC and DC-DC converters. Unfortunately, the use of wide-band III-Nitride (GaN) devices is currently limited mainly to telecom and low-power applications. The lack of high-frequency drivers is one of the factors preventing their application to power converters [4][5]. Modified driver ICs for power Si-MOSFETs are, currently, used to drive the HFET switches, unfortunately, most of them work at relatively low frequencies (below 1MHz) [6][7][8][9]. Few of the driver ICs achieve a switching frequency around 5MHz, but their output impedance characteristics are not compatible with the GaN devices and can lead to unnecessary power loss [10][11][12].

An innovative low power-loss, high-speed drive circuit for GaN power devices was introduced in [4] This work can be considered an adaptation of the driver proposed in [13]. The proposed drive circuit makes GaN devices applicable in power electronics and also makes it possible to fully exploit the advantages of GaN devices, such as superior switching speed and operation in high-power and high-temperature power applications.

The preliminary experimental measurements on a first demonstrator revealed some limitations ascribable to the implementation layout: distorted drive signals, unmatched drive current, long delay time, and rise and fall time [4].

The present paper discusses the improvements in the design and the integrated circuit (IC) implementation. Simulation results show a significant recovery of the overall performances.

II. IC DESIGN CONSIDERATIONS

Fabrication technology for high-speed digital integrated circuits has traditionally sought to reduce the minimum feature size and gate oxide thickness in order to reduce the power supply voltage requirements. However, this trend runs contrary to the demands of the power electronic devices, which typically require much higher supply voltages than those used by digital ICs.

Several existing technologies integrate both, high-voltage (HV) analog and low-voltage (LV) digital circuits, onto a

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single IC chip to achieve miniaturization, high efficiency, reliability, and low cost [14][15]. The proposed design benefits from the use of a cost-effective technique called Smart-Voltage-eXtension (SVX), which implements HV devices in standard CMOS technologies by combining existing layers without modifying the process steps.

The schematic of the entire drive circuit, integrated into a single IC chip, including the level shifters, charge pump, digital block and resonant driver, is reported in Fig.1.

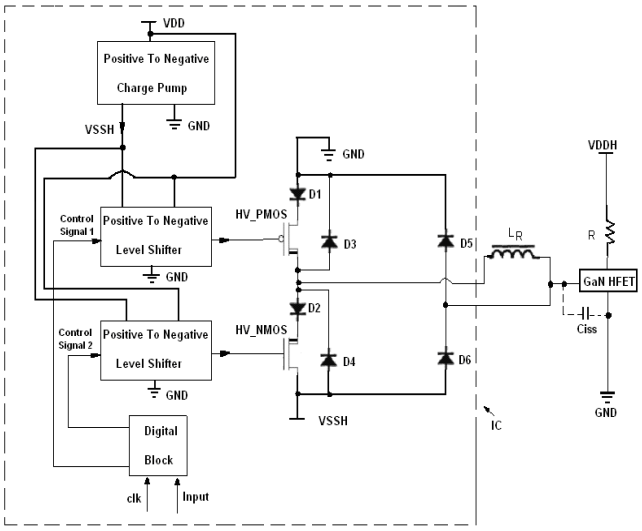

Fig.1. Block of the Integrated Resonant Driver Circuit

Details and analysis of the general operations are fully described in [4]. The charge pump circuit generates the negative high voltage VSSH, requested for the resonant driver, from the positive low-voltage power supply VDD. The digital block converts the 3.3V input signal into two narrow pulse-width control signals. Next, the level shifters change the polarity, with a corresponding increase in the voltage and power level, of the control signals. The amplified signals are used to drive GaN HFETs by means of a resonant small power-switching loss circuit. The resonant topology is constituted by the HV NMOS and HV PMOS connected in totem-pole pair configuration: proper values of the inductance L_R, obtained by adjusting the length of the PCB wire and of C_{iss}, parasitic GaN HFETs capacitance, govern the resonant transition [4].

In the CMOS process, the functions of drain and source on a transistor switch places, so to speak, if the polarity of their voltage changes; as in the resonant driver, in order to avoid improper operation, diodes D1 and D2 have to be connected to the PMOS and NMOS to make them conduct unidirectional. Diodes D3 and D4 are used to form the low-impedance path in order to recover the energy.

The use of the SVX technology in the design of the high-efficiency, negative charge pump and level shifters to obtain high-current, low power-consumption, and high-speed characteristics, represents a critical step in the integration process. In our first tape-out, a 10MHz, 50mA, -7V output voltage driver IC will be fabricated for 100V, 1A GaN devices; the process chosen is H35B4 in Austriamicrosystems.

III. Design of the Two-Stage, Positive-to-Negative Level Shifter for the Drive Circuit

A. Introduction

The GaN HFETs are zero voltage turn-on devices: they require a zero voltage to turn them on and a negative voltage to turn them off. Since the control signals from high-speed digital systems (e.g. FPGA, DSP) are positive, positive-to-negative level shifters are needed to convert a positive signal (which has zero to VDD voltage swing) to a negative signal (which has the voltage swing from zero to VSSH).

Several proposals for level shifters are reported in literature,, but most of them are for positive voltage conversion and they can only change the positive signals to a higher or lower positive voltage level. Only a few level shifters have been proposed to generate a negative voltage level, however, they can only convert the positive signal with a swing of VDD to a signal with a voltage swing from VPP (VPP>=VDD) to VSSH.

Recently a stress-relaxed, negative-voltage level converter has been introduced [16], but unfortunately it is not compatible with the IC processes chosen; the voltage level of the output signals is limited to V_{max}-VDD+V_{tn}+|V_{tp}| (where

V_{max} is the maximum allowable supply voltage), and does not fit our application. A new two-stage, positive-to-negative level shifter is required and it is introduced hereafter in this paper.

B. *The New Two-Stage, Positive to Negative Voltage Level Shifter*

GaN HFETs operations above 10MHz demand a high-speed drive circuit with a 50mA output current consumptions and a -7V output voltage swing. Although HV transistors are available for the IC process chosen, they have lower speed and mostly higher threshold voltage compared to LV transistors.

According to equation (1) for generating a fixed drain current, higher gate-source voltage means much smaller transistor:

$$I_D = \frac{\beta}{2}\frac{W}{L}(V_{GS} - |V_t|)^2 \quad (1)$$

Improvements in the HV transistors switching frequency can be obtained by the use of higher gate-source voltage. Furthermore higher gate-source voltage can also avoid the circuit failure risk due to high threshold voltage of HV transistors.

The schematic of the new two-stage, positive-to-negative level shifter proposed is reported in Fig.2; signal voltage-levels are also shown in the figure.

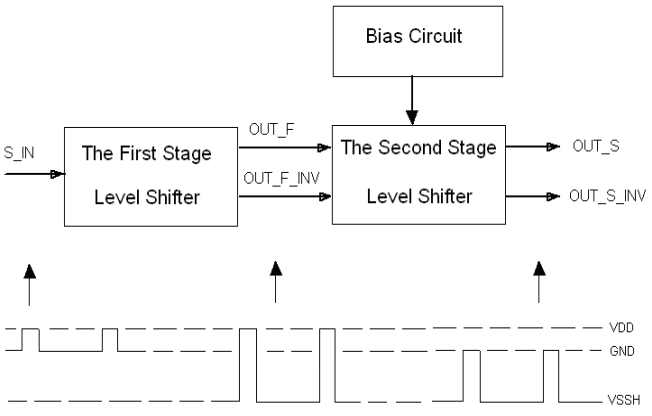

Fig.2. A Two-Stage, Positive-to-Negative Level Shifter

It includes three main parts: a simple low-current level shifter stage for the first stage, a low standby-current level shifter for the second stage, and a bias circuit.

The first stage generates signals with high voltage swing from negative VSSH to positive VDD, and drive the high-current level shifter to increase the switching frequency of the circuit.

The third stage, the bias circuit, provides all the bias voltages and currents for the second stage level shifters.

A brief description of the stages is hereafter reported.

(1) The First Stage of the Level Shifter

The first stage, reported in Fig. 3, comprises two coupled voltage mirrors, M_F2 and M_F1 [14] [17]. The former consists of an HVPMOS (M_F2), together with a low-voltage NMOS (M_F14) connected in a diode configuration as the load. In parallel to M_F14, a pull-down transistor (M_F13) is necessary to drive the output voltage to a high-voltage power supply VSSH in the low state.

The driving signal of the gate of M_F13 must be complementary to VOUT: this is achieved by cross-coupling two voltage mirrors.

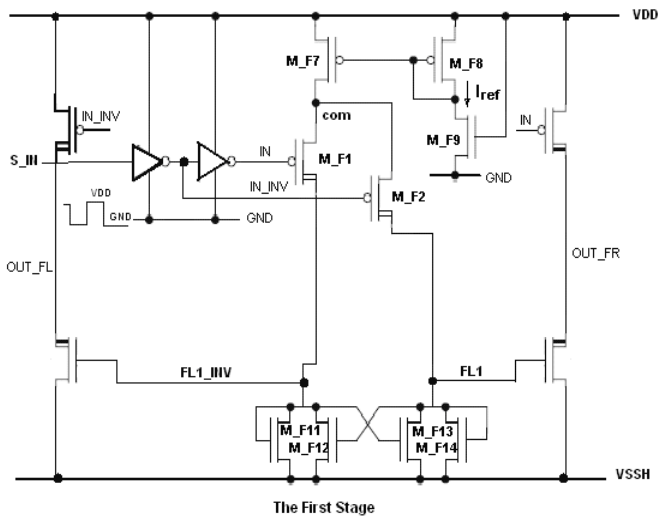

Fig. 3.The First Stage of the Level Shifter

Assuming the output voltage is always low enough to make M_F2 work in the saturation region, the NMOS transistor M_F14, connected as diode, always works in the saturated region.

The current mirror (M_F7, M_F8) is used to generate the current for M_F1 and M_F2. When M_F7 and M_F8 are the

same size, a current equal to I_{ref} will switch between M_F11 and M_F14.

Using three identical NMOS transistors for M_F11, M_F14, and M_F9, the output voltage level of VOUT depends and can be fixed by the current flowing through M_F11 and M_F14.

The possible deviation of the output voltage is given by the tolerance of the low-voltage power supply, according to equation (2):

$$VOUT = VSSH + (\sqrt{\frac{2nI_{ref}}{\beta_n}} + |V_{tn}|) = VSSH + (\sqrt{\frac{2n\frac{\beta_n}{2n}(VDD - |V_{tn}|)^2}{\beta_n}} + |V_{tn}|) = VSSH + VDD \quad (2)$$

Two high-voltage buffers are added to convert VOUT and VOUT_INV to high voltage-swing signals (negative VSSH to positive VDD).

Since the input digital signals are 3.3V, and there is a voltage drop at the current mirror node "com" as shown in Fig.3, in order to guarantee the input transistor operating without dependence on the process variation and to reduce the transistor size for fast switching, low threshold-voltage HV transistors need to be chosen for the input stage of the first stage low-current level shifter.

(2) The Second Stage: Low Standby-Current Level Shifter

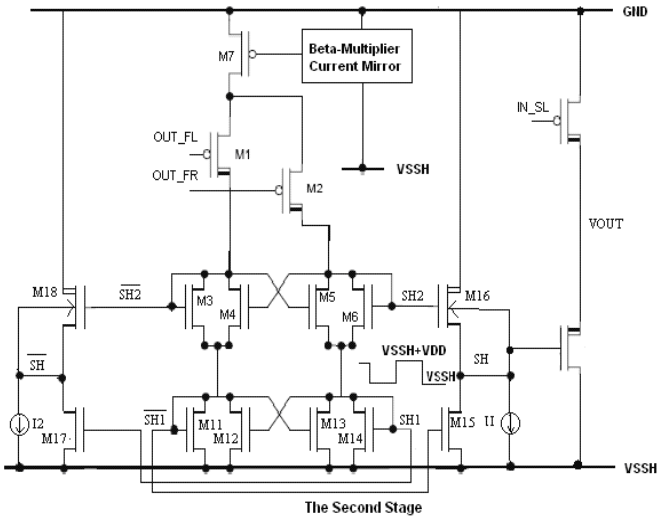

Fig. 4.The Second Stage of the Level Shifter

The second stage of the level shifter is a low standby-current level shifter which generates the GND (0V) to VSSH (-7V) output signals with high output current and low power dissipation. The circuit implements a negative shift-level converter [17]. As shown in Fig. 4, in order to reduce the standby static currents in the circuit, a high-voltage buffer stage is added between the HV NMOS transistor of the output stage and the static level shifter. One of the HV buffer stages is formed by HV source-follower transistor M16, pull-down transistor M15, and the current source I1. The splitting of the cross-coupled pair in the static level-shifter cell maintains the voltage swing at VDD for SH since the voltage level of SH is VSSH+VDD and the voltage level of SH2 must be $(VSSH + VDD + |V_{tn}|)$ [17].

The operation of the circuit is as follows: when $\overline{SH1}$ is active and high, the output is pulled down to VSSH by discharging the gate capacitance of the output NMOS device. When SH2 is active and high, SH is pulled up until M16 enters into weak inversion, thus charging the gate capacitance to VOUT. While the maximum voltage swing of SH is limited to VDD by the static level-shifter cell, its voltage level is maintained at (VSSH+VDD) by the current source I1. The static value of I1 should be close to the minimum current required to keep M16 in weak inversion [17].

The "Beta Multiplier Current Mirror" reported in Fig.4 is used to generate the reference current.

The size of NMOS transistors M3, M6, M11 and M14 needs to be carefully chosen so that the voltage swing of the output signal SH is VDD, according to equation (3):

$$VOUT = VSSH + \left[\sqrt{\frac{2nI_{ref}}{K_n}}\left(\frac{1}{\sqrt{S_6}} + \frac{1}{\sqrt{S_{14}}}\right) + |V_{tn6}| + |V_{tn14}| - |V_{tn16}|\right] \quad (3)$$

The signals SH and $\overline{SH}$ are outputted to high-voltage buffers to generate the signals with voltage swing from VSSH to zero and with increased output current.

IV. Preliminary Results and Conclusions

A full set of simulations has been realized by means of Cadence-Spectre simulator.

Fig. 5 depicts the forecast waveforms for the drive circuit reported in Fig.1.

The input signal S is a 3.3V LV control signal, and the pulse generator changes this signal to two small pulse-width signals S_IN1 and S_IN2 with the same voltage levels.

These two signals are outputted to the two-stage level shifters and transformed into two HV signals S_OUT2 and S_OUT1_B, which have the voltage-swing from -7V to 0V. Finally, these two HV signals are used to drive the PMOS and NMOS transistors of the resonant driver shown in Fig.1, and OUT_DRV is the signal at the gate of the GaN HFET device.

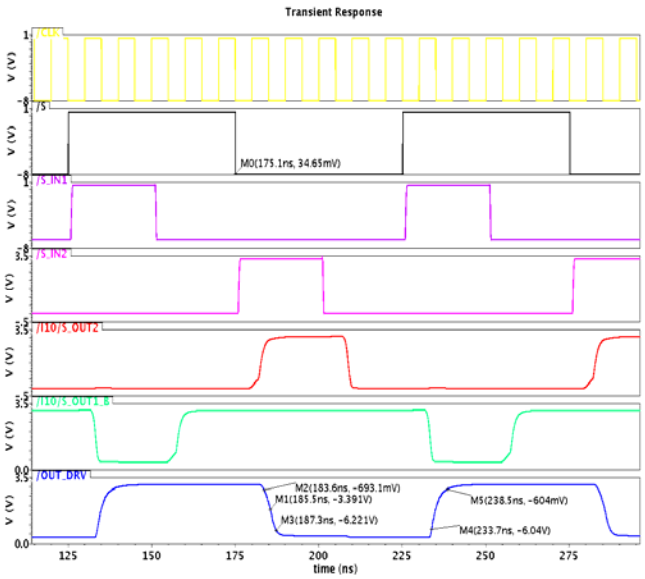

Fig. 5. Simulation Waveforms

The simulation forecasts reveal that the output drive current is about 50mA. The rise time is about 5ns, fall time is nearly 5ns, and delay time is around 10ns.

V. Layout Design and Considerations for the Driver IC Chip

Fig. 6 shows the die floorplan for the driver, which sketches the locations and shapes of the individual cells.

A dedicated layout design is required for ensuring the success and the reliability of IC chips.

Different aspects including matching, ESD, electromigration, etc. need to be taken into account carefully during the layout design.

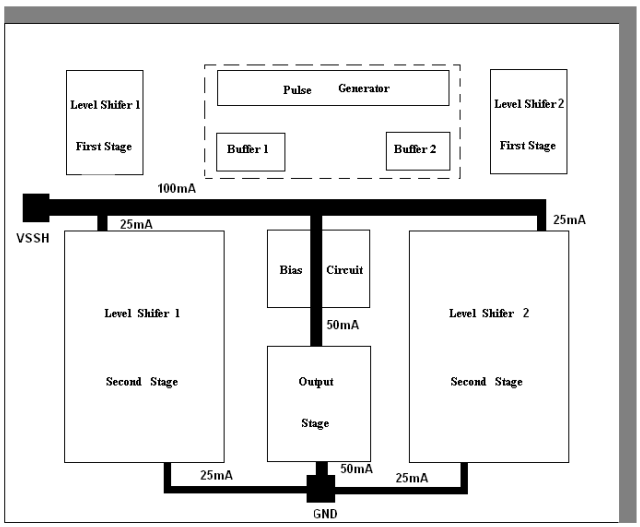

Fig. 6. Layout Floorplan

Three main considerations are described hereafter.

A. *Placements of the cells*

According to Fig.6, the individual cells are represented by rectangles with the appropriate shapes and areas.

Since the driver requires two identical level shifters, the use of mirror-image placements for the cells will have a lot of benefits. First, it will save layout efforts, since same layout can be used for both level shifters. Second, it will ensure that the two level shifters will have good matching between each other and, consequently, similar electrical characteristics [20][21].

B. *Routing of the high-current leads*

The large amount of output current, 50mA, required to drive the GaN HFET devices at 10MHz, forces the use of layout techniques peculiar to high-current circuits. In particular the routing of the high-current leads represents an important aspect for the reliability of the circuit.

Normally, electromigration sets a lower limit on the width of a high-current lead, but metal resistance often forces the use

of much wider leads. In the design all high-current leads should be kept as short as possible to minimize unnecessary metal resistance [21]. Fig. 6 highlights the locations of the high-current leads along with the equivalent DC current they need to conduct.

The proposed locations of the high-current power leads VSSH and GND make sure that these two leads can access all the related cells easily and with short lengths.

C. Layout considerations of the LV digital circuit

As shown in Fig. 6, the digital circuit includes the pulse generator and two buffers in the doted block.

The digital block is powered by the LV power supply, VDD. In order to obtain good isolation between the digital and the analog part of the circuit, we can benefit from the use of one of the facilities of the process H35B4: it is allowed to use floating LV-devices instead of substrate based LV-devices for the LV digital circuit.

This decision is due to the following reasons [15]:

(1) Floating devices are more robust against substrate noise;
(2) Substrate based LV-devices can generate substrate noise;
(3) Substrate based LV-devices can collect substrate currents;
(4) The area penalty for floating logic is negligible;
(5) Substrate based LV-devices need additional layers (Standard NTUB and PTUB) for isolation.

VI. Summary and Future Work

In this paper, the integrated circuit implementation of the diver circuit introduced in [4] for 100V, 1A GaN HFETs switching at 10MHz is described.

The layout design and the implementation process are discussed, underlining the different options settled.

The full set of pre-layout simulation results shown, fully confirm the possibility to exploit the peculiar characteristics of GaN devices.

The design of the IC chip is currently in progress and the chip will be taped out at the end of April 2008.

Acknowledgments

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