OPTOELECTRONIC MULTI-CHIP MODULES

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KEYWORDS: Optical Interconnections, Multi-chip modules, Imaging Fiber Guides

ABSTRACT: In this paper, we present a novel packaging architecture for Optoelectronic Multi-Chip-Modules (OEMCM) based on fiber image guides. Fiber image guides (FIGs) are densely packed lattices of small core fibers that have been traditionally used in medical endoscopes and other remote inspection devices. In our chip packaging architecture, small, rigid segments of FIGs are used to fabricate 3D optical elements with OE chips directly bonded to the outside surfaces. We present several example designs and describe a proof of concept prototype.

INTRODUCTION

As CMOS technology continues to become smaller and faster, connectivity is now a significant limit on the size and complexity of digital systems. The most aggressive commercial multi-chip-module (MCM) packages built to date use over a kilometer of metal interconnect stacked in more than 100 layers of ceramic substrate [1]. These systems have stretched the limits of 2D planar electronic packaging. This paper presents an alternative for next generation systems: 3D optoelectronic-multi-chip-modules (OE-MCM).

The enabling technologies for these packages are large-scale vertical cavity surface emitting laser (VCSEL) arrays[2] and dense flip-chip bonding[3]. Using these technologies it is currently possible to fabricate optoelectronic chips that combine complex logic with large scale optical I/O. There have been several attempts to build systems from these chips using free-space micro and macro optics[4,5]. The success of this approach has been limited by the quality of available diffractive micro-optical elements and by the alignment constraints imposed on a system with multiple chips and complex optics. Guided wave designs have also been proposed based on fiber-per-channel guided wave systems using optical ribbon cable or large core fiber arrays [6]. These systems required accurate alignment between each VCSEL and fiber core.

This paper looks at an innovative alternative OE-MCM architecture based on small, rigid segments of fiber image guides (FIG) [7]. Fiber image guides are densely packed lattices of small core fibers that have been traditionally used in medical endoscopes and other remote inspection systems. They consist of a dense array of small core fibers arranged in a lattice. Fiber diameters typically range from 5 to 20 microns yielding core densities of two thousand to fifteen thousand cores per square millimeter. The relative spatial position of each fiber within the lattice is maintained throughout the length of the bundle. In this context, a 2D array of optical channels is coupled into a segment of FIG and is correspondingly imaged onto the opposite end.

In previous work [8] we have demonstrated that these devices are highly effective for point-to-point links. In these experiments VCSEL and detector arrays have been directly coupled to FIG segments with no additional optical elements in the link. The demonstrates that FIG optics can provide for low component count optical designs that retain the high connection density of free-space architectures but are passively aligned, rugged, and reliable.

In this paper we expand this work to multi-chip MCM design based on small solids fabricated from FIG segments. The OE chips in these designs are based on Silicon on Saphire (SoS) technology using the Peregrine Semiconductor UTSi process. The SoS chips are mixed signal devices that host both CMOS logic and analog CMOS driver and receiver circuits. OE devices, specfically VSCEL and detector arrays, are flip-chip bonded to SoS chip with the devices oriented to transmit and receive through the SoS substrate. Figure one shows a bottom view of an SoS chip with a flip chip bonded detector array. The detectors are clearly visible through the transparent substrate in windows left open

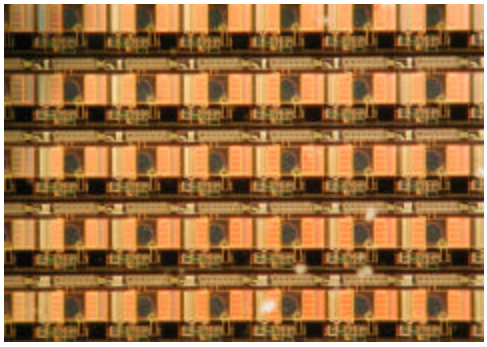

Figure 1: Bottom view of SoS chip showing detector sites

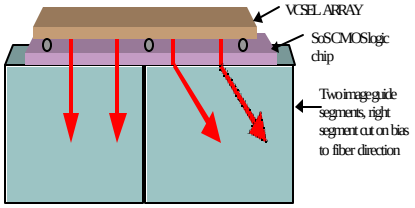

Figure 2: OE chip bonded to fiber bundle segment

during the circuit layout.

These OE chips are directly bonded to the surface of the fiber bundle such that optical signals traverse to transparent SoS substrate and are directly coupled into and FIG as shown in figure 2. In this example there are actually two FIG segments coupled to the OE chip. In the FIG on the left, the fibers are oriented perpendicular to the end surface, on the right the segment is cut such that the fiber angle is at a bias. This angular coupling is possible because FIGs typically have a significantly higher numerical aperture than communications fibers. We will exploit this characteristic to implement spatial fanout and it is the basis for our muli-chip interconnect implementations.

It is also important to note that since the OE are transparent and are directly bonded to the FIG surface, there are several advantages to these designs when compared to other types of chip-level optical interconnections. Most significant is the fact that the rigid fiber bundle segments become both the structural elements of the package and the and the communication channels. Since all parts of the systems are directly bonded to one another, the package is far more tolerant to thermal and mechanical stress. There are no global alignment constraints. Each device needs only to be aligned to the package. Since the OE chips and the package are transparent, the devices can be passively aligned. Finally, as a 3D implementation the package can be designed for minimun size and time of flight latency.

MULTI-CHIP PACKAGE ARCHITECTURE

To support OE-MCM's of size greater that two chips, it is necessary to provide a spatial fan-out and fan-in mechanism whereby each chip can communicate with multiple partners. Our approach is based on the spatial partitioning of the channels within a VCSEL/detector array. Specifically, segments of rigid fiber bundle, shown in the foreground of figure 3, are cut at various angles relative to the fiber propagation direction. These pieces are side-bonded, as shown in the background of the figure, such that one end forms a planar surface on with an OE-chip can be mounted. The other ends become spatially separated which is the basis of our fan-out mechanism. A VCSEL/detector array on the planar surface is partitioned into regions based on the layers of FIGs bonded at the planar end. Each region provides for bi-directional communications through one of the cut bundles and delivers spatial separated signals at the other surface. Although this example is of little use in MCM architectures, figures 4 and 5 show examples extruded polygon shapes that are the basis for four and six chip MCMs.

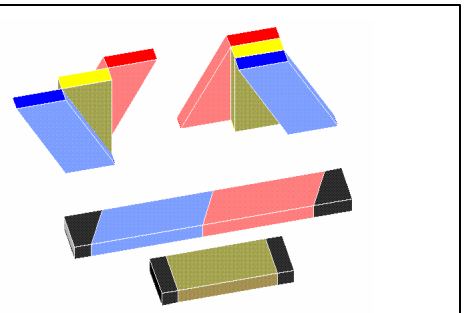
Figure 3: Spatial fan-out mechanism

There are a number of ways in which to scale these MCM to larger numbers chips. The first is to simply increase the number of sides to the polygon formed in each slice. We have arbitrarily chosen a limit of 45 degrees as the maximum insertion angle for all structures. Given this limit, the interconnection graph for any OE-MCM built from an n-sided polygon stack will always connect each chip to (n/2)+1 devices on the opposite side of the device.

An alternative scaling method is to increase the size of each stack such that the interconnection pattern is repeated every N layers (or layer pairs).

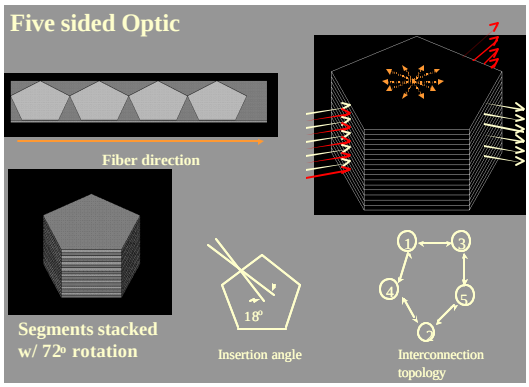

Figure 4: five-sided MCM optic

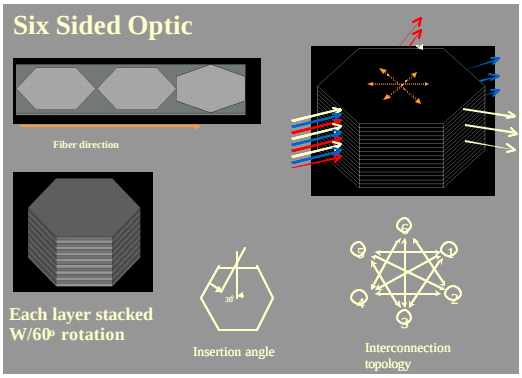

Figure 5: six-sided MCM optic

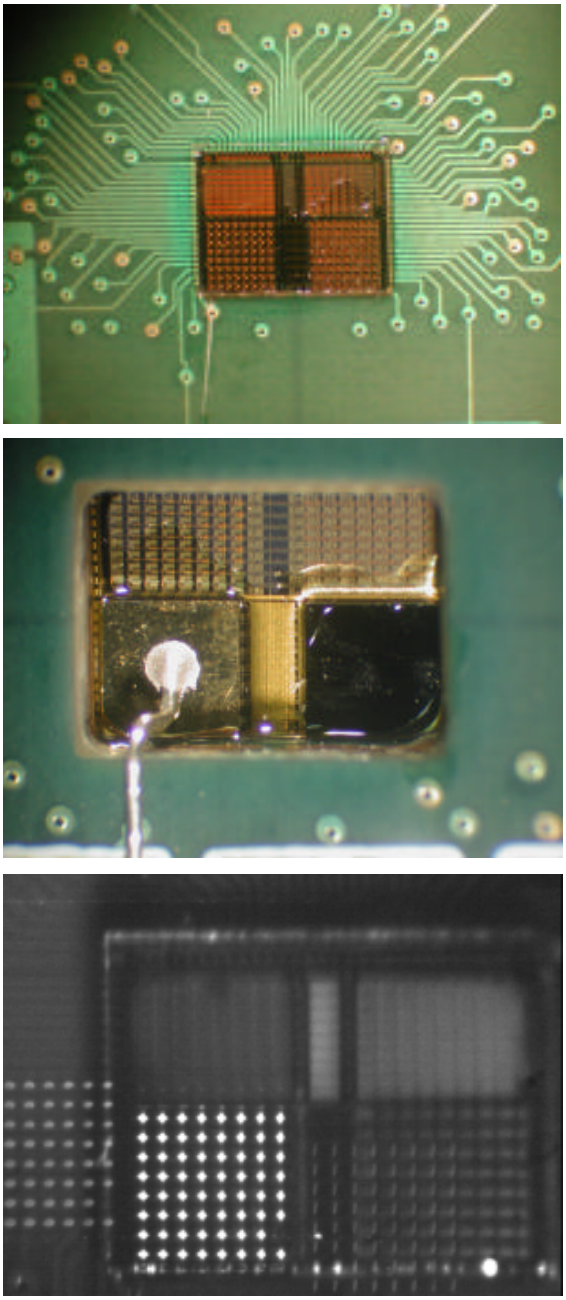

Fig. 6. Photographs of 64 channel transceiver/switch chip designed at the University of Pittsburgh and fabricated by Peregrine. (Top) The chip is shown bump-bonded (upside-down) to the board. PIN-photodiode and VCSEL chips are bonded to the opposite site. (Middle) The chip is shown through the board cavity, exposing the PIN-photodiode and VCSEL chips. (Bottom) View from the bottom of the chip with VCSELs turned on.

DEMONSTRATOR SYSTEM DESIGN

Our demonstrator system consists of a 3-chip OE-MCM that makes up a 64 channel switch fabric. Each chip implements eight independent 8x8 switching elements. The three chips are connected in a 3 stage non-blocking butterfly network. The chips measure 4mm x 5.5mm and were fabricated part of the Peregrine ultra-thin silicon-on-sapphire (UTSi) COOP run. Each switch chip implements 8, 8x8, switches in CMOS logic, as well as 64 channel (8x8) driver and receiver arrays. Switch configuration information is stored in a two-level memory. The "map" level of the configuration memory drives the configuration of the switch logic. The "cache" level is a second copy of the configuration loaded externally through the electrical interface. To conserve I/O pins the cache level is loaded over multiple cycles of a 12-bit I/O bus. Once a new configuration is completely loaded into the cache, the switch configuration is set in a single parallel transfer between the cache and map level memory. We found that this switch configuration mechanism is consistent with most commercially available state-of-the-art crossbar switch modules. Each switch element is an 8-to-1 multiplexor with registers that hold the "cache" and "map" switch configuration data for each output. Additional logic for loading and decoding the configuration data is distributed throughout the logic section. Alignment marks were created using the top metal layer and placed throughout the chip to facilitate alignment when bonding the dies to the optic. This is possible due to the optical transparency of the die substrate. Figure 6 are images of the switch chip, bump-bonded to both an 8x8 PIN photodiode chip and an 8x8 VCSEL chip. The switch logic is shown on the top half of the die. After the photodetector and VCSEL chips are bump bonded to the switch chips, the resulting OE chips were then bonded directly to an optical element built from two segments of rigid fiber image guides. These fiber bundles guide all of the optical signals between the chips without additional optical elements. Optical input and output is implemented with a pair of 2D (8x8) fiber ribbon cables that are also directly bonded to the image guide optic. Electrical connections are made via bump bonds between the UTSi devices and conventional printed circuit boards on which the MCM is mounted.

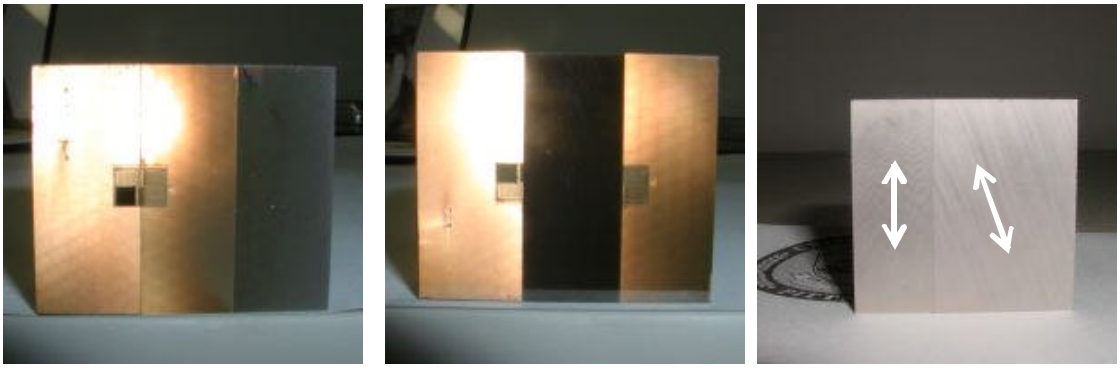

Fig 7. Images of optic with one switch chip mounted on the top, shown from the top, bottom, and side.

MCM ARCHITECTURE

At the core of the MCM architecture is an optical element built by bonding together two rigid segments of imaging fiber guide. These image guides are produced by Schott Fiber Optics and consist of a dense array of small core fibers arranged in a lattice. Fiber diameters typically range from 5 to 20 microns, yielding core densities of two thousand to fifteen thousand cores per square millimeter. Thus, an array of optical channels imaged on one surface is correspondingly imaged on the opposite surface. It is important to keep in mind that this is an imaging operation. Each optical channel is spatially over-sampled by multiple fiber cores. This is not a core-per-channel arrangement such as you have in a fiber ribbon cable. For the OE-MCM design presented in this paper, OE chips are directly bonded to the end surface of the fiber bundle such that optical signals traverse to transparent silicon-on-sapphire substrate and are coupled into the fiber guide. Since the fiber bundle segments are rigid, the waveguides become both the structural elements and the communication channels. As can be seen by Figure 7, a chip is mounted on a two section fiber image guide. The left half of the chip is on top of the section where the fibers run orthogonal to the chip surface. The right half of the chip is on top of the section where the fibers run 70 degree off the chip surface. This is shown in the bottom view of the fiber image guide. The side view of the optic shows the fiber direction. Figure 8 is a wireframe view of the system that depicts the three OE-chips and 2D fiber arrays mounted on the image guide optic. Note that the optic is built from two segments that are distinguished by the orientation of the internal fibers shown by the dotted lines. In the smaller segment, the fibers in the image guide run vertically and are normal to the imaging surfaces. In the larger segment, shown below Chip #2, the image guide is cut such that the fibers run at a 20 degree offset. This offset is required because the location of the VCSEL and detector arrays on the switch-chips is not symmetrical relative to the chip axis. The required orientation of the arrays in chip #2 places the switching logic between the arrays and the fiber ferrule. This introduces an offset relative the arrays in chips #1 and #3 that is compensated by the bias in the fiber direction. Note that chip #1 and chip #3 are turned by ninety degrees relative to the fiber ferrule and chip on the top surface. These corner-turns implement spatially the interconnection pattern for the 3-stage CLOS network. As shown in this diagram, optical signals enter the switch via one of fiber ribbons and traverse the vertically cut image guide to the detector array on chip #1. Signals are switched by row to particular VCSEL on chip #1 where they re-enter image guide optic, this time in the 20 degree bias cut segment. This segment images the signals on the detector array of chip #2 which

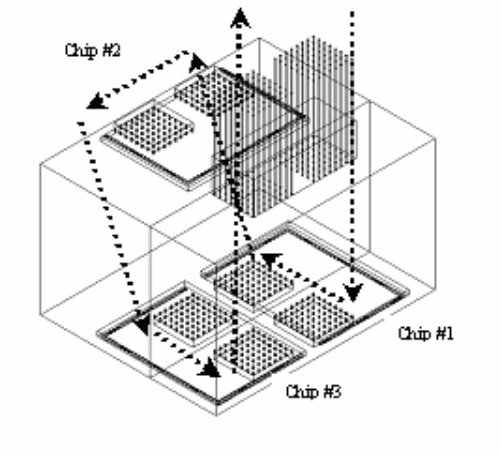

Fig. 8. Wireframe view of switch architecture.

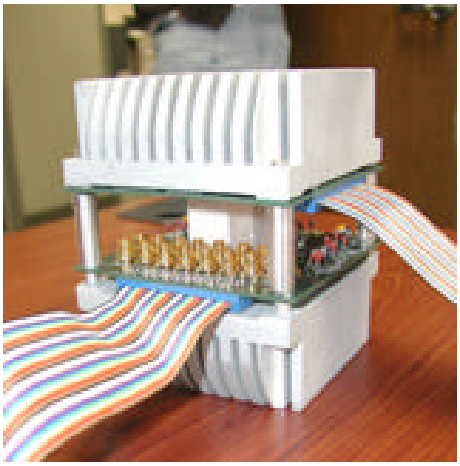

Fig. 9. OE-MCM demonstrator

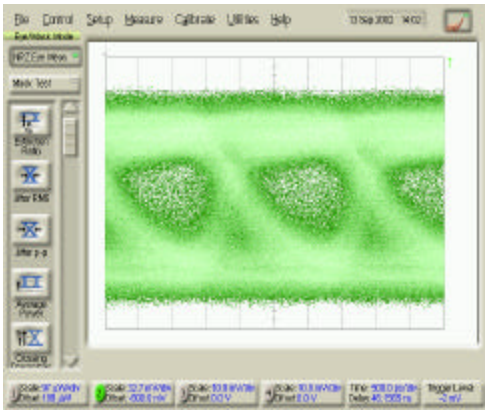

Fig 10. 500Mhz eye diagram for probed operation of the circuit. This shows receiver output for an optical signal that was coupled out of a FIG.

performs the second stage switching operation after which the signals re-enter the bias cut segment. Chip #3 performs the final switching operation to direct the signal to output fiber channel. The signal enters the outgoing ferrule through the vertically cut image guide between chip #3 and the output ferrule. Note that chip #1 and chip #3 are turned by ninety degrees relative to the fiber ferrule and chip on the top surface. These corner-turns implement spatially the interconnection pattern for the CLOS network. The completed package \ for the demonstrator system is shown in Figure 9. \

CONCLUSIONS AND FUTURE WORK

We have demonstrated a novel multi-chip-module architecture for chip level optical interconnection based on fiber image guide technology.. These structures appear to hold a great deal of promise for supporting large scale low-latency chip-level interconnections that are rugged and easily manufactured.

We are currently in the process of fabricating and characterizing a proof of concept prototype. In this prototype we are testing some of basic technology for image guide based OE/MCM devices.

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