Optoelectronic Multi-Chip-Module Implementation of a 64-Channel Fiber Switch

Jason D. Bakos, Donald M. Chiarulli, and Steven P. Levitan
Departments of Computer Science and Electrical Engineering
University of Pittsburgh
Pittsburgh, PA 15260
jbakos@cs.pitt.edu, don@cs.pitt.edu, steve@ee.pitt.edu

ABSTRACT

We present a demonstration prototype of an optoelectronic 3-chip OE-MCM module that implements a 64-channel non-blocking fiber optic switch. Each OE-switch-chip was implemented using Peregrine UTSI technology flip-chip bonded to VCSEL and photodetector arrays that support 64 channels of optical input and output that are guided within the MCM by a optic built from two segments of image guide.

Keywords: Optical Inteconnections, Multi-chip modules, Imaging Fiber Guides

Introduction

In recent publications [1,2] we have proposed a novel design for optoelectronic multi-chip-modules (OE-MCM) based on small segments of rigid imaging fiber bundles. We have shown that these designs have significant advantages over conventional electronic MCM's and over free-space optical MCM's including compact device geometry, relaxed alignment constraints, and a highly manufacturable monolithic packaging architecture.

In this paper we report on our ongoing work in this area. Specifically, the design and implementation of a 64 channel non-blocking fiber optic switch that is packaged in a 3-chip OE-MCM based on this technology. The switch chips were built as part of the recent Peregrine UTSi COOP run that is currently in fabrication. Separate, 8x8 VCSEL and PIN-photodiode arrays will be flip-chip bonded to these devices. The resulting OE chips will in turn be bonded directly to an optical element built from two segments of rigid fiber image guides. These fiber bundles guide all of the optical signals between the chips without additional optical elements. Optical input and output in implemented with a pair of 2D (8x8) fiber ribbon cables that are also directly bonded to the image guide optic. Electrical connections are made via wire bonds between the UTSi devices and conventional printed circuit boards on which the MCM is mounted. The entire MCM uses a volume of less the one cm^3.

Switch Chip Design

This section outlines the design of the OE switching chip. There are three such chips in the 64 channel switch fabric. Each chip implements eight independent 8x8 switching elements and the ensemble of three chips are connected in a 3 stage non-blocking CLOS network as shown in Figure 1. Each column in the switching network is implemented by one switching chip as shown by the labels in the figure.

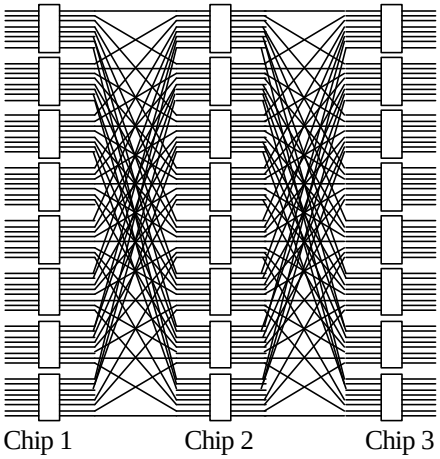


Figure 1: Switch Architecture and Chip Level Partitioning

An image of the switch-chip layout is shown in figure 2. The chip measures 4mm x 5.5mm and is being fabricated in the Perregrine .5um UTSi process. Simulation data suggests that the chip will operate at 2 Gb/s NRZ. In an examination of the layout one can easily distinguish four regions in chip topology. The lower left and right quadrants are 8x8 arrays of receiver and driver logic respectively. The upper quadrants are the switch logic. The switch logic implements a set of

8x8 crossbar switches such that the receivers in each column of the receiver array are connected to the drivers in the corresponding column of the driver array.

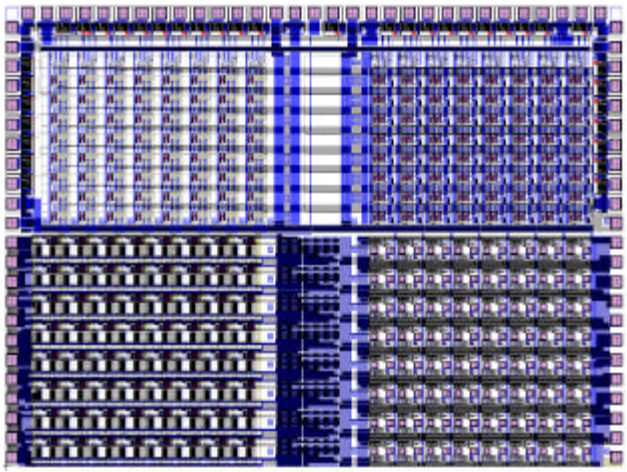


Figure 2: Switch Chip Layout

The switch is configured electrically and requires 192 bits of configuration data. This information is stored in a two-level configuration memory. The "map" level of the configuration memory drives the configuration of the switch logic. The "cache" level is a second copy of the configuration loaded externally through the electrical interface. To conserve I/O pins the cache level is loaded over multiple cycles of a 12-bit I/O bus. Once a new configuration is completely loaded into the cache, the switch configuration is set in a single parallel transfer between the cache and map level memory.

MCM architecture

At the core of the MCM architecture is an optical element built by bonding together two rigid segments of imaging fiber guide. Theses image guides are produced by Schott Fiber Optics and consist of a dense array of small core fibers arranged in a lattice. Fiber diameters typically range from 5 to 20 microns, yielding core densities of two thousand to fifteen thousand cores per square millimeter. Thus, an array of optical channels imaged on one surface is correspondingly imaged on the opposite surface. It is important to keep in mind that this is an imaging operation. Each optical channel is spatially over-sampled by multiple fiber cores. This is not a core-per-channel arrangement such as you have in a fiber ribbon cable.

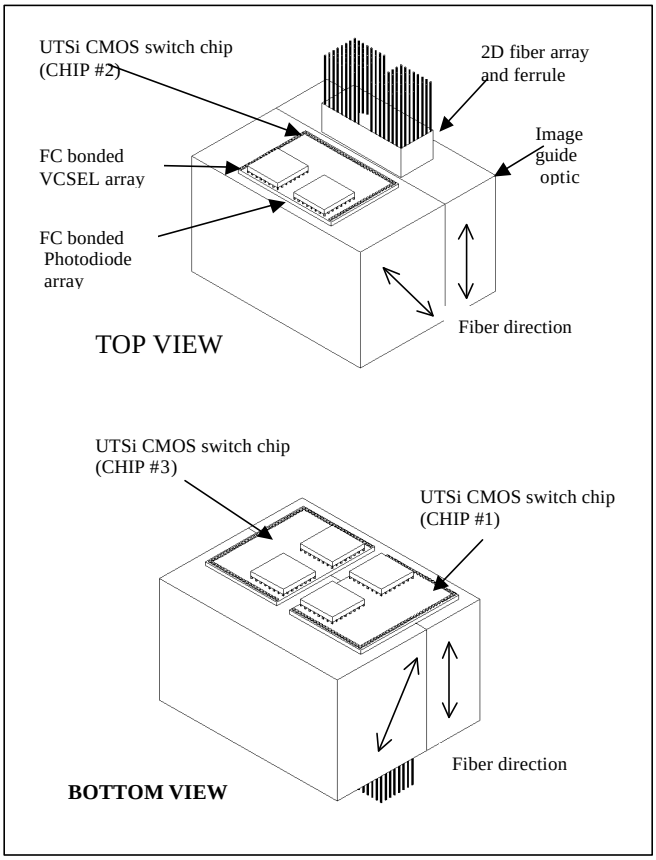
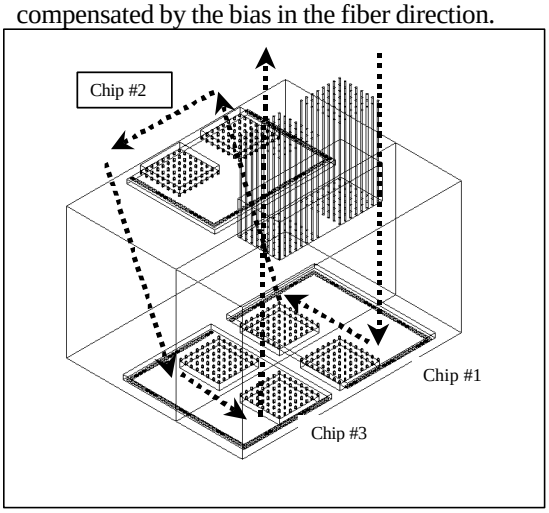


Figure three is a pair of line drawings showing top and bottom views for the OE-MCM with electrical connections omitted. These views depict the three OE-chips and 2D fiber arrays mounted on the image guide optic. Note that the optic is built from two segments that are distinguished by the orientation of the internal fibers shown by the arrows one the side of each drawing. In the smaller segment, shown below the fiber ferrule in the top view, the fibers in the image guide run vertically and are normal to the imaging surfaces. In the larger segment, shown below Chip #2 in the top view, the image guide has be cut such that the fibers run at a 20 degree offset. This offset is required because the location of the VCSEL and detector arrays on the switch-chips is not symmetrical relative to the

chip axis. The required orientation of the arrays in chip #2 places the switching logic between the arrays and the fiber ferrule. This introduces an offset relative the arrays in chips #1 and #3 that is compensated by the bias in the fiber direction.



In the bottom view drawing note that chip #1 and chip #3 are turned by ninety degrees relative to the fiber ferrule and chip on the top surface. These corner-turns implement spatially the interconnection pattern for the CLOS network shown in Figure 1.

Figure 4 is wireframe view of the OE-MCM with bold-dotted lines added to trace the signal paths through the switch. As shown in this diagram, optical signals enter the switch via one of fiber ribbons and traverse the vertically cut image guide to the detect array on chip #1. Signals are switched by row to particular VCSEL on chip #1 where they re-enter image guide optic, this time in the 20 degree bias cut segment. This segment images the signals on the detector array of chip #2 which performs the second stage switching operation after which the signals re-enter the bias cut segment. Chip #3 performs the final switching operation to direct the signal to output fiber channel. The signal enter the outgoing ferrule through the vertically cut image guide between chip#3 and the output ferrule.

Conclusions and Future Work

In this prototype we are testing some of basic technology for image guide based OE/MCM devices. The interconnect for this case is fairly simple using only two image guide segments and two sides of the 3D fiber structure. As we reported in our previous publications, devices of significantly higher dimensions and chip count are possible. Our intention is to implement one of these structures in a more complex application, such as processor to memory interconnection.

References

1. D. Chiarulli, S. Levitan, P. Derr, R. Hofmann, B. Greiner, and M. Robinson, "**Demonstration and Characterization of Multi-Channel Interconnections Using Imaging Fiber Bundles Butt Coupled to Optoelectronic Devices**", *Applied Optics* , Vol. 39, No. 5, pp. 698 - 703, (10 February 2000).

2. D. M. Chiarulli, S. P. Levitan, M. Robinson, C. Cryan, "**Optoelectronic Multi-Chip Modules Based on Imaging Fiber Bundle Structures**," Optics in Computing (OC 2000) Quebec City, Canada, June 18-23, 2000.