Optoelectronic Multi-Chip Module Demonstrator System

Jason D. Bakos[1], Donald Chiarulli[1], Steven P. Levitan[2]
Departments of Computer Science[1] and Electrical Engineering[2], University of Pittsburgh
jbakos@cs.pitt.edu, don@cs.pitt.edu, steve@ee.pitt.edu

Abstract: We present our work on a demonstration prototype of an optoelectronic 3-chip OE-MCM that implements a 64-channel non-blocking fiber optic switch.

Keywords: Optical Interconnections, Multi-chip modules, Imaging Fiber Guides

OCIS codes: (130.0250) Optoelectronics, (110.2350) Fiber optics imaging

1. Introduction

In previously published work [1, 2, 3, 4, 5], we have presented a number of link architectures that demonstrate both short haul (multi-chip module) and board-to-board interconnection technology. We have shown that these designs have significant advantages over both conventional electronic MCM's and free-space optical MCM's, such as compact device geometry, relaxed alignment constraints, and a highly manufacturable monolithic packaging architecture. In this paper, we report our progress in constructing and characterizing a prototype for optoelectronic multi-chip-modules (OE-MCM). This prototype is a demonstration application that implements a 3-chip, 64-channel non-blocking fiber optic switch. The packaging and interconnect for this demonstrator is based on the use of small segments of rigid imaging fiber bundles.

2. Switch Chip Design

Our demonstrator system consists of a 3-chip OE-MCM that makes up a 64 channel switch fabric. Each chip implements eight independent 8x8 switching elements. The three chips are connected in a 3 stage non-blocking CLOS switch network. The chips measure 4mm x 5.5mm and were fabricated part of the Peregrine ultra-thin silicon-on-sapphire (UTSi) COOP run. Each switch chip implements 8, 8x8, switches in CMOS logic, as well as 64 channel (8x8) driver and receiver arrays. Switch configuration information is stored in a two-level memory. The "map" level of the configuration memory drives the configuration of the switch logic. The "cache" level is a second copy of the configuration loaded externally through the electrical interface. To conserve I/O pins the cache level is loaded over multiple cycles of a 12-bit I/O bus. Once a new configuration is completely loaded into the cache, the switch configuration is set in a single parallel transfer between the cache and map level memory. We found that this switch configuration mechanism is consistent with most commercially available state-of-the-art crossbar switch modules. Each switch element is an 8-to-1 multiplexor with registers that hold the "cache" and "map" switch configuration data for each output. Additional logic for loading and decoding the configuration data is distributed throughout the logic section. Alignment marks were created using the top metal layer and placed throughout the chip to facilitate alignment when bonding the dies to the optic. This is possible due to the optical transparency of the die substrate. Figure 1 is an image of the switch chip, bump-bonded to both an 8x8 PIN photodiode chip and an 8x8 VCSEL chip. The switch logic is shown on the left half of the die. This image also shows the optical transparency of the sapphire die substrate. After the photodetector and VCSEL chips are bump bonded to the switch chips, the resulting OE chips were then bonded directly to an optical element built from two segments of rigid fiber image guides. These fiber bundles guide all of the optical signals between the chips without additional optical elements.

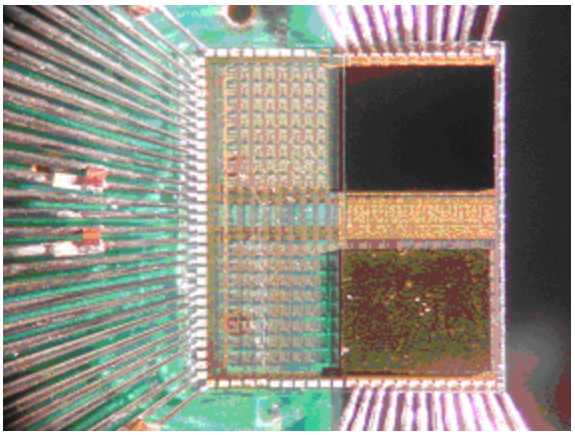

Fig. 1. Photograph of 64 channel transceiver/switch chip designed at the University of Pittsburgh and fabricated by Peregrine. 8x8 PIN detector and VCSEL arrays are shown flip-chip bonded to the device.

Optical input and output is implemented with a pair of 2D (8x8) fiber ribbon cables that are also directly bonded to the image guide optic. Electrical connections are made via bump bonds between the UTSi devices and conventional printed circuit boards on which the MCM is mounted.

3. MCM architecture

At the core of the MCM architecture is an optical element built by bonding together two rigid segments of imaging fiber guide. These image guides are produced by Schott Fiber Optics and consist of a dense array of small core fibers arranged in a lattice. Fiber diameters typically range from 5 to 20 microns, yielding core densities of two thousand to fifteen thousand cores per square millimeter. Thus, an array of optical channels imaged on one surface is correspondingly imaged on the opposite surface. It is important to keep in mind that this is an imaging operation.

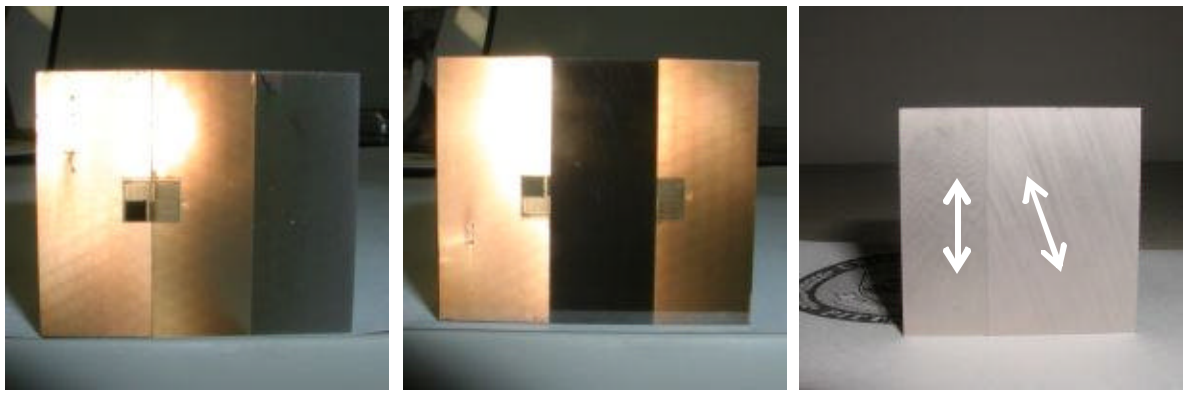

Fig 2. Images of optic with one switch chip mounted on the top, shown from the top, bottom, and side.

Each optical channel is spatially over-sampled by multiple fiber cores. This is not a core-per-channel arrangement such as you have in a fiber ribbon cable. For the OE-MCM design presented in this paper, OE chips are directly bonded to the end surface of the fiber bundle such that optical signals traverse to transparent silicon-on-sapphire substrate and are coupled into the fiber guide. Since the fiber bundle segments are rigid, the waveguides become both the structural elements and the communication channels. As can be seen by Figure 2, a chip is mounted on a two section fiber image guide. The left half of the chip is on top of the section where the fibers run orthogonal to the chip surface. The right half of the chip is on top of the section where the fibers run 70 degree off the chip surface. This is shown in the bottom view of the fiber image guide. The side view of the optic shows the fiber direction. Figure 3 is a wireframe view of the system that depicts the three OE-chips and 2D fiber arrays mounted on the image guide optic. Note that the optic is built from two segments that are distinguished by the orientation of the internal fibers shown by the dotted lines. In the smaller segment, the fibers in the image guide run vertically and are normal to the imaging surfaces. In the larger segment, shown below Chip #2, the image guide is cut such that the

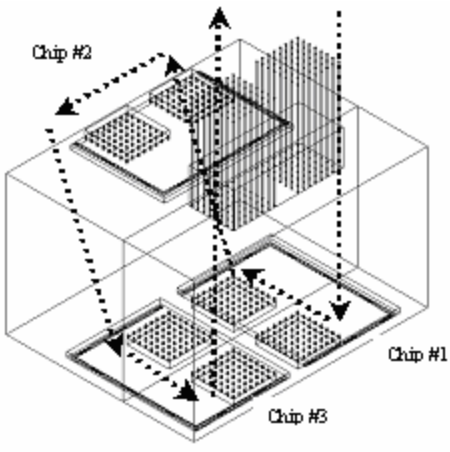

Fig. 3. Wireframe view of switch architecture.

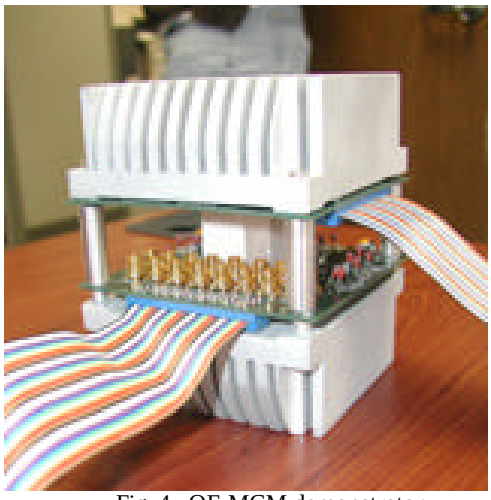

Fig. 4. OE-MCM demonstrator

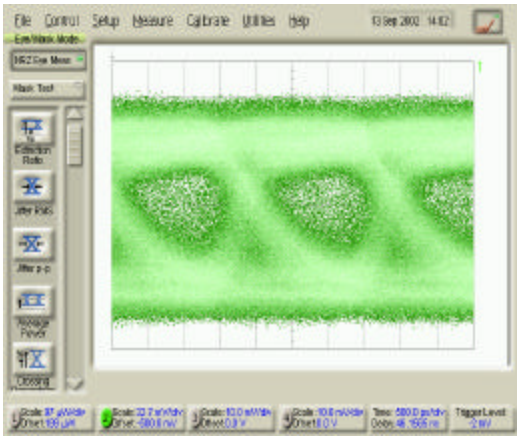

Fig 5. 500Mhz eye diagram for probed operation of the circuit. This shows receiver output for an optical signal that was coupled out of a FIG.

fibers run at a 20 degree offset. This offset is required because the location of the VCSEL and detector arrays on the switch-chips is not symmetrical relative to the chip axis. The required orientation of the arrays in chip #2 places the switching logic between the arrays and the fiber ferrule. This introduces an offset relative the arrays in chips #1 and #3 that is compensated by the bias in the fiber direction. Note that chip #1 and chip #3 are turned by ninety degrees relative to the fiber ferrule and chip on the top surface. These corner-turns implement spatially the interconnection pattern for the 3-stage CLOS network. As shown in this diagram, optical signals enter the switch via one of fiber ribbons and traverse the vertically cut image guide to the detector array on chip #1. Signals are switched by row to particular VCSEL on chip #1 where they re-enter image guide optic, this time in the 20 degree bias cut segment. This segment images the signals on the detector array of chip #2 which performs the second stage switching operation after which the signals re-enter the bias cut segment. Chip #3 performs the final switching operation to direct the signal to output fiber channel. The signal enters the outgoing ferrule through the vertically cut image guide between chip #3 and the output ferrule. Note that chip #1 and chip #3 are turned by ninety degrees relative to the fiber ferrule and chip on the top surface. These corner-turns implement spatially the interconnection pattern for the CLOS network. The completed electrical and mechanical tester OE-MCM for the demonstrator system is shown in Figure 4. The ribbon cables are used to configure the three switch chips. Large heat sinks are used to dissipate the heat generated by the switch chips and the voltage regulators on the printed circuit boards.

4. Test Results and Current Status

To date we have probe tested the receiver and transmitter section of the device using a test mode configuration of the switching logic that drives outputs directly from the configuration memory and accesses the receiver output on a test pad. Both inputs and outputs were directly coupled through the image guide optic during this test. The eye diagram in Figure 5 shows the test results for one channel output at 500MHz. The bandwidth limitation is primarily due to limitations on the probing system. We anticipate that the system will operate at 1-2 Gbs when bonded to PCB boards.

5. References

1. D. M. Chiarulli, S. P. Levitan, M. Wisser, "Optoelectronic Multi-Chip-Modules Using Fiber Optics Components," Glass and the Photonics Revolution at the Annual Conference of the German Society of Glass Technology, Bad Soden, Germany, May 28-29, 2002.
2. Jason D. Bakos, Donald M. Chiarulli, and Steven P. Levitan, "Optoelectronic Multi-Chip-Module Implementation of a 64-Channel Fiber Switch," 2002 International Topical Meeting on Optics in Computing 2002. pp 161-163.
3. Donald M. Chiarulli, Steven P. Levitan, Matt Robinson, and Karim Tatah, "Optoelectronic Multi-Chip Modules Based on Imaging Fiber Bundle Structures," in Optics in Computing, OSA Technical Digest (Optical Society of America, Washington DC, 2001), pp. 125-127.
4. D. M. Chiarulli, S. P. Levitan, M. Robinson, C. Cryan, "Optoelectronic Multi-Chip Modules Based on Imaging Fiber Bundle Structures," Optics in Computing (OC 2000) Quebec City, Canada, June 18-23, 2000.
5. D. Chiarulli, S. Levitan, P. Derr, R. Hofmann, B. Greiner, and M. Robinson, "Demonstration and Characterization of Multi-Channel Interconnections Using Imaging Fiber Bundles Butt Coupled to Optoelectronic Devices", Applied Optics , Vol. 39, No. 5, pp. 698 - 703, (10 February 2000).