Integrated Circuit Implementation for a GaN HFET Driver Circuit

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***Abstract*—This paper presents the design and implementation of a new integrated circuit (IC) that is suitable for driving the new generation of high-frequency GaN HFETs. The circuit, based upon a resonant switching transition technique, is first briefly described and then discussed in detail, focusing on the design process practical considerations. A new level-shifter topology, used to generate the zero and negative gate–source voltages required to switch the GaN HFET, is introduced and analyzed. The experimental measurements included in this paper report the results of tests carried out on an IC designed and fabricated as part of the multiproject die in high-voltage process H35B4 of Austriamicrosystems. They fully demonstrate the performance of the proposed driver that opens the possibility of fully exploiting the wide capabilities and advantages of GaN devices for use in power electronics applications.**

***Index Terms*—GaN HFET, gate driver integrated circuit (IC), high frequency.**

I. Introduction

THE rapidly developing research on wide-band III-nitride semiconductor materials (such as GaN) has been driven by the unique properties of these materials, making the III-nitride technology a promising approach for high-power, high-temperature, high-speed, and high-efficiency applications [1]–[3]. Although these devices can be extremely useful in industrial power electronics applications and improve the efficiency and the regulation of ac–dc and dc–dc converters, the lack of high-frequency drivers is one of the key factors preventing their spread. At the present, the use of wide-band III-nitride (GaN) devices is limited mainly to telecom and low-power applications [4]–[6]. Currently available driver integrated circuits (ICs) designed for power Si-MOSFET can be adapted to drive GaN HFET devices, but the relatively low switching frequencies reached (below 1 MHz) cut the advantage in commercial apparatus [7]–[10]. Few of them achieve higher frequency, around 5 MHz, but with output impedance characteristics not suitable for the GaN devices. This incompatibility leads to unnecessary power loss that makes impossible their adoption in high-efficient compact applications. [11]–[13].

The authors introduced a novel, innovative, low-power-loss, and high-speed drive circuit for GaN power devices [4], [14]. The proposed driver circuit makes it possible to fully exploit the advantages of the superior switching frequency of GaN devices and allow their use in high-power high-temperature power electronics applications.

The preliminary experimental measurements based upon a first demonstrator built with discrete components revealed some limitations that are ascribable to the implementation layout: distorted drive signals, unmatched drive current, long delay time, and rise and fall times [4], [14].

A chip recently fabricated in an Austriamicrosystems high-voltage (HV) CMOS process, according to a design performed by the authors, shows a significant recovery of the overall characteristics up to 10 MHz. This paper describes the improvements in the design and discusses the IC implementation realized at the Microelectronics Laboratory of the University of South Carolina. The experimental results are discussed in the following sections.

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II. Description of the Drive Circuit for GaN HFETs

The HFET devices are zero-voltage switch-on devices; in other words, they need to be driven by a zero voltage to turn on and by a negative voltage to turn off. This unconventional requirement in the driving characteristics has represented further difficulties in the design and fabrication of a 10-MHz IC to drive 100-V 1-A GaN HFET devices with $V_G = -7$ V at 50 mA. The basic schematic of the circuit proposed by the authors is shown in Fig. 1 [5], [14], [15].

The drive circuit is based upon resonant switching transition techniques by means of an LC tag, a totem-pole pair, and two diodes to recover part of the energy back into the voltage source in order to reduce the power loss [4], [14]. As shown in Fig. 1, the control signals at the input are processed by the digital block which can convert, by means of a control signal generator, a

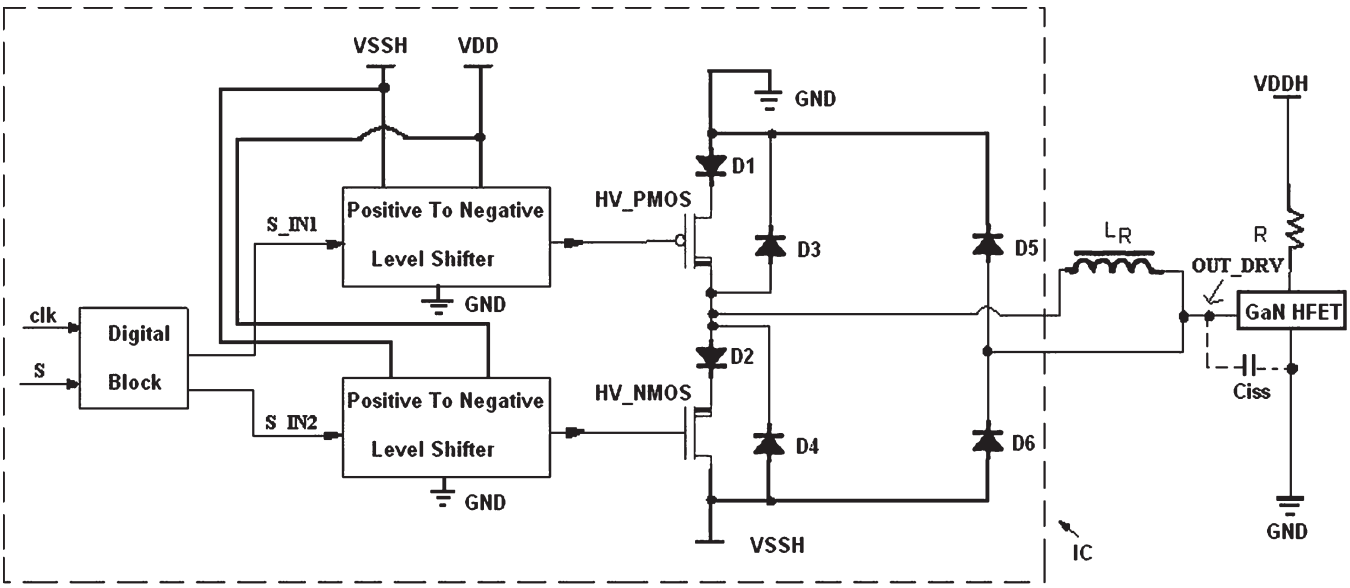


Fig. 1. Block of the integrated resonant driver circuit.

low-voltage (LV) digital input signal (3.3 V) into two narrow pulsewidth control signals or directly use two external small pulsewidth signals as the inputs for the level shifter depending on the need of the users. The level shifters change the polarity of the control signals with a corresponding increase in the voltage and power level. The amplified signals are used to drive GaN HFETs by means of a resonant drive circuit. The resonant topology is constituted by the HV NMOS and HV PMOS connected in a totem-pole pair configuration, diodes, inductor L_R, and the input capacitor $C_{\rm iss}$ of GaN HFETs.

The driver IC needs two external power supplies: 3.3 and -7 V. In the applications, several methods can be utilized to generate the -7-V power supply from the 3.3-V power supply:

1) isolated dc/dc power converter;
2) charge pump.

In the future, a charge pump circuit will be built into the driver IC so that only one external power supply will be needed for the chip.

The proposed drive circuit, specifically designed for GaN HFETs, highlights several advantages as listed in the following.

1) The use of a smart resonant topology, with effective energy recovery, reduces the power loss of the circuit. The low-impedance path of the resonant circuit minimizes the conduction losses. The two small pulsewidth input signals avoid the cross-conduction of the PMOS and NMOS in the totem-pole pair, allowing a further reduction of the power loss of the circuit. The resonant inductor limits the switching power loss by slowing down the increase of the drain current of the GaN device, which decreases the overlap between the drain current I_D and the drain–source voltage $V_{\rm DS}$ [4], [14].
2) Proper values of the inductance L_R could be obtained by adjusting the length of the PCB wire between the driver and the power devices and allow the circuit to operate free of magnetic components.
3) The level shifter changes the polarity and increases the voltage level and drive capability of the input signals.
4) The voltage-clamped commutation makes the circuit high tolerant to the timing variation of the control signals.

Although the first prototype was affected by some limitation due to parasitic and unoptimized layout, the design of the IC driver allowed one to cope with these problems [4], [14].

The realization of a mixed-signal IC required a critical selection of the best suited microelectronic technology. Fabrication technology for high-speed digital ICs has traditionally sought to reduce the minimum feature size and gate-oxide thickness in order to reduce the power supply voltage requirements. However, this trend runs contrary to the demands of the power electronics devices, which typically require much higher supply voltages than those used by digital ICs developed in CMOS technology. Several existing technologies integrate both HV analog and LV digital circuits onto a single IC chip to achieve miniaturization, high efficiency, reliability, and low cost [17], [18]. All the standard CMOS processes available in MOSIS can only work at 5 V or lower. We chose the HV process H35B4 from Austriamicrosystems for the design proposed in this paper. H35B4 is a cost-effective technique called Smart Voltage eXtension (SVX), which implements HV devices in standard CMOS technologies by combining existing layers without modifying the process steps.

III. Design of the Positive-to-Negative Level Shifter for the Drive Circuit

A. Introduction

One of the main difficulties that prevented the realization of the driver for GaN HFETs has been the interfacing of the zero-to-positive control signals coming from high-speed digital systems (e.g., field-programmable gate array (FPGA) and DSP) and the zero-to-negative voltage required to switch the device. Suitable high-power positive-to-negative level shifters

are needed to convert a positive signal (which has a zero-to-VDD voltage swing) to a negative signal (which has a voltage swing from zero to $VSSH$, a high negative voltage level).

Several proposals for level shifters are reported in the literature, but most of them are for positive voltage conversion and are specifically devoted to change the positive signals to a higher or lower positive voltage level. Only a few level shifters consider the generation of negative voltage levels, and however, they can only convert the positive signal with a swing of VDD to a signal with a voltage swing from VPP ($VPP >= VDD$) to $VSSH$ [17], [19] (where VPP is a positive voltage).

Recently, a stress-relaxed negative voltage level converter has been introduced [20], but unfortunately, the voltage level of the output signals is limited to $V_{\max} - VDD + V_{\rm tn} + |V_{\rm tp}|$ (where $V_{\max}$ is the maximum allowable supply voltage; $V_{\rm tn}$ and $V_{\rm tp}$ are the threshold voltages for the NMOS and PMOS transistors, respectively), and it is not compatible with the SVX technology.

In order to allow an easy IC integration, a new positive-to-negative level shifter that is suitable for converting input signals to zero-to-negative voltages is introduced in the following section.

B. Two-Stage Positive-to-Negative Voltage Level Shifter

GaN HFET operations above 10 MHz demand a high-speed drive circuit with a 50-mA output current consumptions and a -7-V output voltage swing. Although HV transistors are available for the IC process chosen, they have lower speed and mostly higher threshold voltage compared to LV transistors. According to (1), for generating a fixed drain current, higher gate–source voltage means much smaller transistor. The smaller the size of the transistor, the smaller the input capacitance that the transistor will have. Consequently, improvements in the HV transistor switching frequency can be obtained by the use of higher gate–source voltage

$$I_D = \frac{uC_{\rm ox}}{2}\frac{W}{L}\left(V_{\rm GS} - |V_t|\right)^2 \tag{1}$$

where

$V_{\rm GS}$	gate–source voltage of the transistor;
μ, μ_n, and μ_p	effective, electron, and hole mobilities, respectively;
$C_{\rm ox}$	gate-oxide capacitance per unit area;
W	width of the transistor;
L	length of the transistor;
V_t	threshold voltage of the transistor;
I_D	drain current of the transistor.

In order to take advantage of this property, a new two-stage positive-to-negative level shifter is designed. The first stage is in charge of changing the voltage level of the input signals, while the second stage is focusing on increasing the drive capability of the signals. Fig. 2 shows the schematic of the basic building block reproducing the level shifter proposed, as well as the signal voltage levels.

The inputs of the level shifter are digital control signals with a 3.3-V voltage swing coming from the digital block. In order to make this level-shifter cell work at high frequencies,

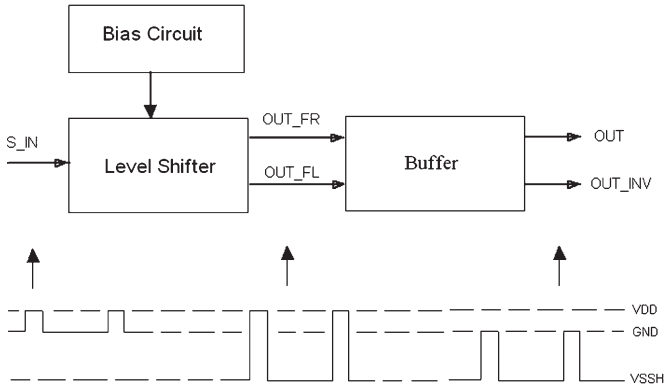


Fig. 2. Block diagram of the new positive-to-negative level shifter.

a low-current level-shifter cell is chosen as the first stage, which generates signals with HV swing from negative $VSSH$ to positive VDD. An auxiliary bias circuit is required in order to provide the bias currents for the level-shifter cell.

The second stage of the drive circuit has been selected in order to change the voltage swing and, at the same time, increase the drive capability of the circuit (high output current) and minimize the power dissipation. These specifications were set to satisfy the requirements of the high-frequency commutation for the GaN HFET switch. In the first design [5], a low-standby-current level shifter was considered for the second stage. The choice was forced by the need of avoiding the use of 50-V MOS transistors from Austriamicrosystems IC library that limited the performances, particularly high speed, required for the driver. Few months later, in the middle of 2008, Austriamicrosystems released new 20-V PMOS and NMOS transistor cells with improved performances than the old 50-V transistor series. This library upgrade opens the possibility to reconsidering the use of a buffer approach for the second stage.

1) GaN HFET High-Frequency Circuit Driver Based Upon the New Level-Shifter Cell: Fig. 3 shows the two-stage driver circuit implementing the new positive-to-negative level-shifter cell.

Bias circuit: A current mirror topology is used to bias the level-shifter cell. The reference current is generated by means of three transistors: M_F7, M_F8, and M_F9. The size of M_F9 is adjusted to obtain the required reference current $I_{\rm ref}$ calculated approximately by using

$$\begin{aligned} I_{\rm ref} &= \frac{\beta_n(\text{M\_F9})}{2n}\left(V_{\rm GS}(\text{M\_F9}) - V_{\rm tn}\right)^2 \\ &= \frac{\beta_n(\text{M\_F9})}{2n}(VDD - V_{\rm tn})^2 \end{aligned} \tag{2}$$

where $\beta_n = \mu_n * C_{\rm ox} * W/L$ and VDD is the positive LV power supply.

If the transistors M_F7 and M_F8 are matched, a current equal to $I_{\rm ref}$ will switch between M_F11 and M_F14 by turning on and off the input transistors M_F1 and M_F2.

Description of the new level-shifter cell: The new level-shifter cell proposed comprises two coupled voltage mirrors, M_F2 and M_F1 [17], [21]–[23]. The former consists of an HV PMOS (M_F2), together with an LV NMOS (M_F14) connected in a diode configuration as the load. In parallel to

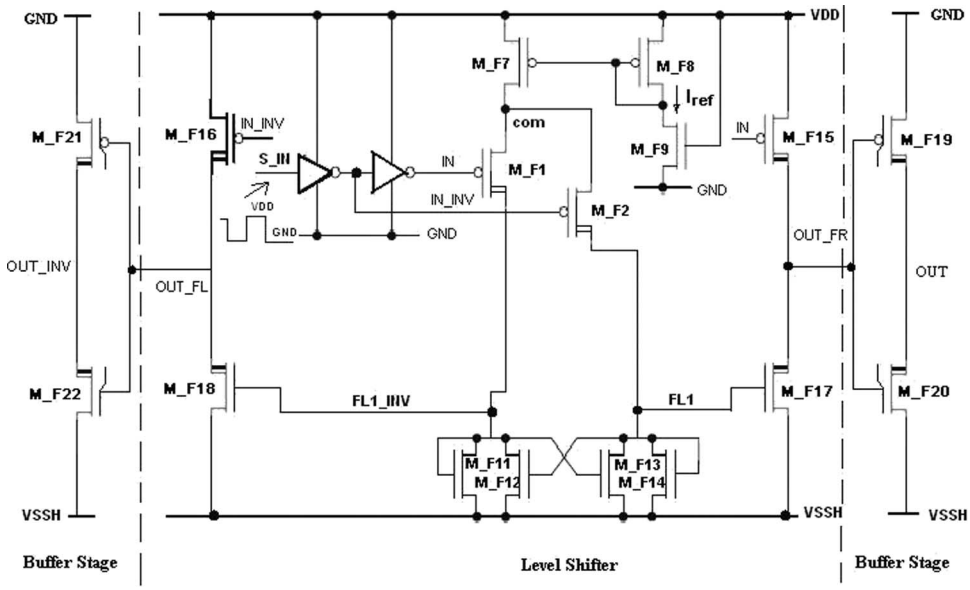


Fig. 3. Schematic of the new positive-to-negative basic level-shifter cell.

M_F14, a pull-down transistor (M_F13) is necessary to drive the output voltage to an HV power supply $VSSH$ in the low state. The driving signal of the gate of M_F13 must be complementary to FL1: This is achieved by cross-coupling two voltage mirrors.

Assuming that the output voltage is always low enough to bias M_F2 in the saturation region, the NMOS transistor M_F14, connected as diode, always works in the saturated region. Choosing the same size for transistors M_F7 and M_F8, the current flowing through transistor M_F14 ($I_{\mathrm{M\_F14}}$), which is calculated by (3), will be equal to I_{ref}.

$$\begin{aligned} I_{\mathrm{M\_F14}} &= \frac{\beta_n(\mathrm{M\_F14})}{2n}\left(V_{\mathrm{GS}}(\mathrm{M\_F14}) - V_{\mathrm{tn}}\right)^2 \\ &= \frac{\beta_n(\mathrm{M\_F14})}{2n}\left(V(\mathrm{FL1}) - VSSH - V_{\mathrm{tn}}\right)^2 \end{aligned} \quad (3)$$

where $VSSH$ is the negative power supply.

Since $I_{\mathrm{M\_F14}} = I_{\mathrm{ref}}$, solving (3), we obtain the output voltage for signal FL1, shown as

$$V(\mathrm{FL1}) = VSSH + \sqrt{\frac{2nI_{\mathrm{ref}}}{\beta_n(\mathrm{M\_F14})}} + V_{\mathrm{tn}} \quad (4)$$

where I_{ref} is the reference current generated by the bias circuit.

Solving (2) and (4), the following equation is obtained:

$$\begin{aligned} V(\mathrm{FL1}) &= VSSH + \sqrt{\frac{2nI_{\mathrm{ref}}}{\beta_n}} + V_{\mathrm{tn}} \\ &= VSSH + \sqrt{\frac{2n\frac{\beta_n(\mathrm{M\_F9})}{2n}(VDD - V_{\mathrm{tn}})^2}{\beta_n(\mathrm{M\_F14})}} + V_{\mathrm{tn}}. \end{aligned} \quad (5)$$

Using three identical NMOS transistors for M_F11, M_F14, and M_F9, in other words, considering that they have the same β_n, the output voltage level of FL1 and FL1_INV can be fixed by the current flowing through M_F11 and M_F14. The possible deviation of the output voltage is given by the tolerance of the LV power supply, according to

$$\begin{aligned} V(\mathrm{FL1}) &= VSSH + \sqrt{\frac{2n\frac{\beta_n(\mathrm{M\_F9})}{2n}(VDD - V_{\mathrm{tn}})^2}{\beta_n(\mathrm{M\_F14})}} + V_{\mathrm{tn}} \\ &= VSSH + \sqrt{\frac{2n\frac{\beta_n}{2n}(VDD - V_{\mathrm{tn}})^2}{\beta_n}} + V_{\mathrm{tn}} \\ &= VSSH + VDD. \end{aligned} \quad (6)$$

In reality, the voltage swing of the output signals will be affected by other factors such as matching of transistors M_F11, M_F14, and M_F9, matching between transistors M_F7 and M_F8, etc. However, this kind of deviation can be reduced to be very small by a good layout design.

The low level of the input digital signals (3.3 V) and the voltage drop at the current mirror node "com," as shown in Fig. 3, make critical the choice of the input transistor in the stage. In order to guarantee the correct operation of the circuit and to minimize the transistor size for fast switching, low threshold-voltage HV transistors have been chosen for the input stage of the first-stage low-current level shifter. As shown in Fig. 3, most transistors in the circuit are LV transistors. In addition, the current of the circuit is low, and only two small-size HV transistors are required for the input transistors: All these characteristics make the circuit suitable for high-frequency operations.

Two HV buffers composed of a pair of thin gate-oxide PMOS and NMOS are added to convert FL1 and FL1_INV to high voltage swing signals, OUT_FR and OUT_FL, which have a voltage swing from negative $VSSH$ to positive VDD.

An improved level-shifter cell, which eliminates the turn-on failure risk of the input transistors or is specifically designed for low-power dissipation, can be used to substitute the basic

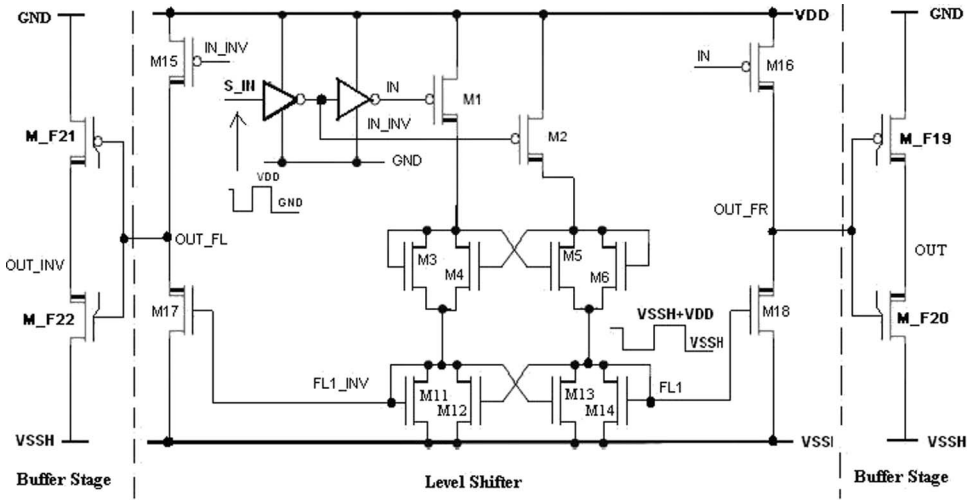


Fig. 4. Improved basic level-shifter cell.

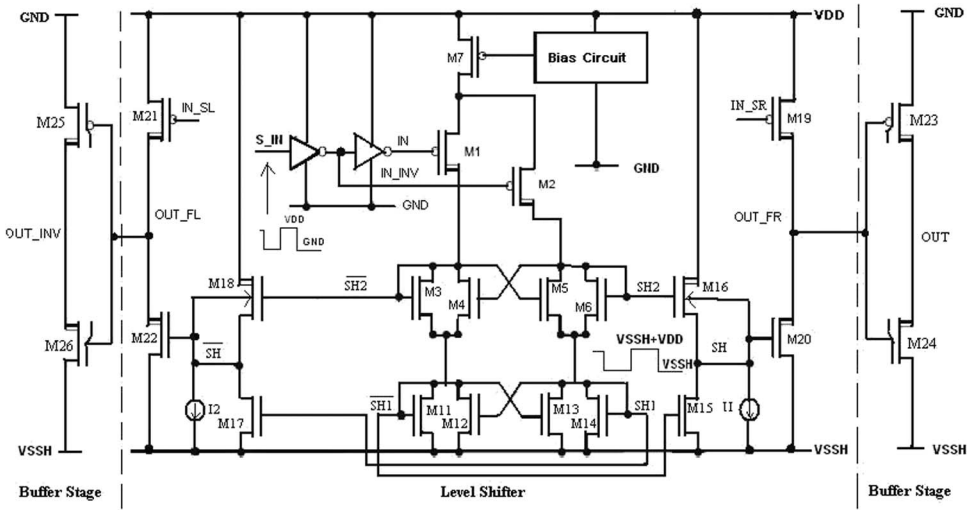


Fig. 5. Second low-standby-current level-shifter cell.

level-shifter cell in Fig. 3. These approaches are described in Section III-B2 and B3.

HV buffer stage: An HV buffer stage, which works under the voltage $VSSH$ and GND, is added after the first-stage level-shifter cell to change the voltage level and the drive capability of the control signals. The buffer stage is composed of a pair of thick gate-oxide PMOS transistor M_F19/M_F21 and NMOS transistor M_F20/M_F22. According to (1), for obtaining a specific value of output current, higher gate–source voltage means smaller transistor sizes, so higher operation speed. The sizes of the transistors and the stages of the buffer can be adjusted according to the required drive current and speed. Consequently, this buffer stage with high gate–source voltage increases the drive capability of the signals and maintains a high operation frequency at the same time.

2) Improved Level-Shifter Cell: As described in (1), in Fig. 3, the low input voltage levels and the voltage drop at the point "com" make the selection of the input transistors M_F1 and M_F2 critical and also affect the safe operation of the circuit since the threshold voltages of the HV input transistors are usually high. In order to avoid the risk of failure, an improved level shifter was designed. Fig. 4 shows the schematic of the improved basic level shifter.

As shown in Fig. 5, the current mirror is removed in this level shifter. The sources of the input transistors are directly connected to the positive power supply VDD to eliminate the turn-on failure risk due to the voltage drop at "com" and the large threshold voltages of the input transistors. The cross-coupled pair splits up into two parts in order to obtain a voltage swing from $VSSH$ to $VSSH + VDD$ for FL1 and FL1_INV and to maintain a voltage drop as low as possible across the splitting voltage mirror pair so that the input transistors always work at the saturation region and LV transistors can be used in the voltage mirror to obtain high operation speed. However, the sizes for all the transistors in this circuit need to be carefully selected to obtain the required output voltage and current. Furthermore, it should be mentioned that this circuit is sensitive to process variations.

3) Level-Shifter Stage Based Upon the Low-Standby-Current Level-Shifter Cell: Fig. 5 shows the two-stage driver circuit implementing the low-standby-current positive-to-negative level-shifter cell [21]. An HV buffer stage is added between the

HV NMOS transistor of the output stage and the static level shifter in order to reduce the standby static currents in the circuit. One of the HV buffer stages is formed by HV source-follower transistor M16, pull-down transistor M15, and the current source I1. The splitting of the cross-coupled pair in the static level-shifter cell maintains the voltage swing at VDD for SH since the voltage level of SH is $VSSH + VDD$ and the voltage level of SH2 must be $(VSSH + VDD + |V_{\rm tn}|)$ [21].

A brief description of the operation of the circuits is in what follows: When $\overline{\rm SH1}$ is active and high, the output is pulled down to $VSSH$ by discharging the gate capacitance of the output NMOS device. When SH2 is active and high, SH is pulled up until M16 enters into weak inversion, thus charging the gate capacitance to OUT. While the maximum voltage swing of SH is limited to VDD by the static level-shifter cell, its voltage level is maintained at $(VSSH + VDD)$ by the current source I1. The static value of I1 should be close to the minimum current required to keep M16 in weak inversion [21].

For this stage, the same bias circuit used in Fig. 3 is chosen for the low-standby-current level shifter. The voltage swing of the output signal SH can be calculated by

$$V({\rm SH}) = VSSH + \left[\sqrt{\frac{2nI_{\rm ref}}{K_n}}\left(\frac{1}{\sqrt{S_6}} + \frac{1}{\sqrt{S_{14}}}\right) + |V_{\rm tn6}| + |V_{\rm tn14}| - |V_{\rm tn16}|\right] \quad (7)$$

where $S = W/L$; $K_n = \mu n * C_{\rm ox}$; S_6, S_9, S_{14}, and S_{16} are the S parameters for transistors M_F6, M_F9, M_F14, and M_F16, respectively; and $V_{\rm tn6}$, $V_{\rm tn9}$, $V_{\rm tn14}$, and $V_{\rm tn16}$ are the threshold voltages for transistors M_F6, M_F9, M_F14, and M_F16, respectively.

By solving (2) and (7)

$$\begin{aligned} V({\rm SH}) &= VSSH \\ &\quad + \left[\sqrt{\frac{2n\frac{K_nS_9}{2n}(VDD - V_{\rm tn9})^2}{K_n}}\left(\frac{1}{\sqrt{S_6}} + \frac{1}{\sqrt{S_{14}}}\right) + |V_{\rm tn6}| + |V_{\rm tn14}| - |V_{\rm tn16}|\right] \\ &= VSSH \\ &\quad + \left[(VDD - V_{\rm tn9}) * \sqrt{S_9} * \left(\frac{1}{\sqrt{S_6}} + \frac{1}{\sqrt{S_{14}}}\right) + |V_{\rm tn6}| + |V_{\rm tn14}| - |V_{\rm tn16}|\right]. \end{aligned} \quad (8)$$

Three NMOS transistors with identical type and size are chosen for M_F6, M_F14, and M_F16, and an NMOS transistor of the same type and with 1/4 size is used for M_F9; we get $V_{\rm tn6} = V_{\rm tn14} = V_{\rm tn16} = V_{\rm tn9} = V_{\rm tn}$ and $S_9 = 1/4 * S_6 = 1/4 * S_{14} = 1/4 * S$. By solving (8), a voltage swing of VDD can be obtained by the low-standby-current level shifter, as shown in the following equation:

$$\begin{aligned} V({\rm SH}) &= VSSH + \left[(VDD - V_{\rm tn}) * \sqrt{S/4} * \left(\frac{1}{\sqrt{S}} + \frac{1}{\sqrt{S}}\right) + |V_{\rm tn}| + |V_{\rm tn}| - |V_{\rm tn}|\right] \\ &= VSSH + VDD. \end{aligned} \quad (9)$$

The same HV buffer stage described in Section III-B1 is used to convert SH to an HV signal OUT which has a voltage swing from $VSSH$ to GND.

4) Comparison of the Level Shifters and Design Considerations: In our newly designed chip, two different topologies have been separately implemented for the first stage: a basic positive-to-negative level-shifter cell and an improved basic level-shifter cell, introduced in Section III-B1 and B2 by the authors. The different design approaches of the different level-shifter cells allow the comparison of the performances of the efficiency and of the cost of the driver circuit. Here, we report the major results of the comparison.

1) Performance. All the level shifters meet the general requirements to drive GaN devices at 10 MHz. However, the higher number of transistors in the low-standby-current level shifter produces larger parasitic capacitances in the circuit, which leads to lower speed and worse performance compared to the basic level shifter.
2) Power dissipation. The low-standby-current level shifter has much lower power dissipations than the proposed level shifter since it is specially designed to reduce the standby current, so to reduce the dissipated power in the circuit.
3) Circuit design complexity. The low-standby-current level shifter is more complicated than the basic level shifter. It has eight more transistors in the cell and two more bias circuits to provide reference currents I1 and I2 as shown in Fig. 5. When we do the layout design for the low-standby-current level-shifter cell, there are more aspects which we need to take care of in order to obtain good performance, such as match between more transistors.
4) Cost. The low-standby-current level shifter, due to the added transistors and circuits, requires a larger die size and, consequently, is more expansive.

The voltage swing and output current required for the level shifter in our application are not too high (7 V and 10 mA). This limits the benefit of the low-standby-current level shifter in Section III-B3, which is specifically devoted to very high efficient solutions. The performance, circuit complexity, and cost are aspects of paramount importance in this specific design, and they make the basic level-shifter cell and the improved basic level-shifter cell introduced in Section III-B1 and B2, respectively, more suitable for the design.

IV. Simulation Results

A full set of simulations has been realized by means of Cadence-Spectre simulator. Fig. 6 shows the forecast waveforms of both the drive circuits shown in Fig. 1 for the solutions

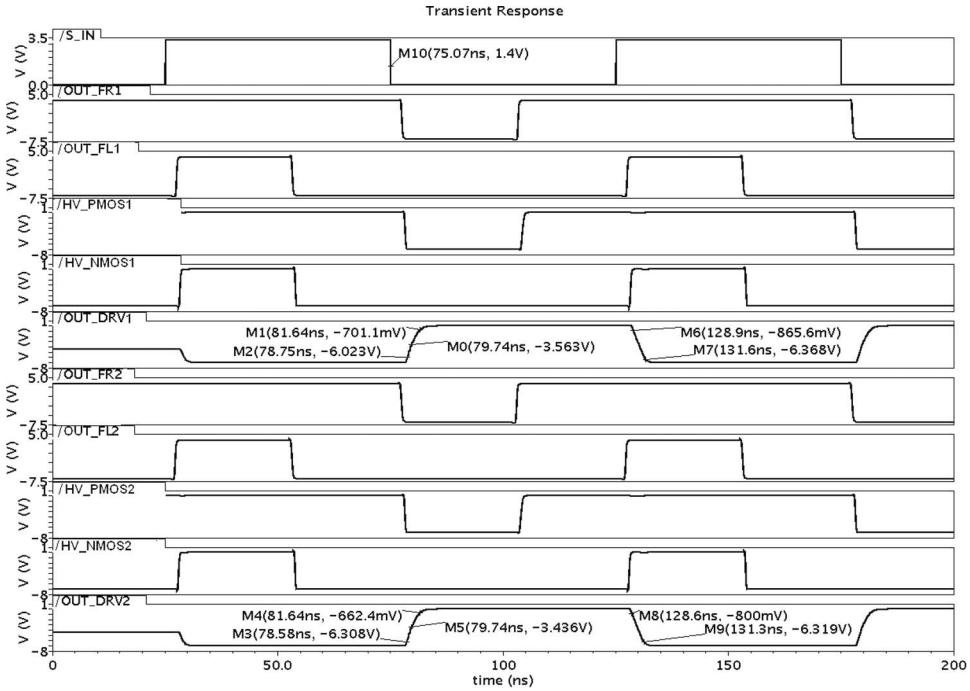


Fig. 6. Simulation waveforms.

described in Figs. 3 and 4. Driver circuit 1 is the driver with the basic level shifter shown in Fig. 3, and Driver circuit 2 is the driver with the improved basic level shifter shown in Fig. 4. The waveforms with denotations 1 and 2 report the signals for Driver circuits 1 and 2, respectively.

In Fig. 6, the input signal S_IN is an external 3.3-V LV control signal, and the pulse generator changes this signal to two small pulsewidth signals (OUT_FL1/2 and OUT_FR1/2) with the same voltage levels. These small pulsewidth signals are output to the two-stage level shifters and transformed into two HV signals HV_PMOS1/2 and HV_NMOS1/2, which have the voltage swing from −7 to 0 V. Finally, these two HV signals are used to drive the HV PMOS and NMOS transistors of the resonant driver shown in Fig. 1, and OUT_DRV1 and OUT_DRV2 are the output drive signals from the driver circuit, which are used to drive the GaN HFET devices. The loads for both of the drive circuits are capacitors which have a comparable value with the input capacitance of the GaN devices targeted to drive. In this specific simulation, the load capacitance is 20 pF. Both of the drive circuits provide a 50-mA output drive current. Fig. 6 shows the waveforms for both of the drivers at operation frequency of 10 MHz. As shown in Fig. 6, the simulation forecasts reveal that both Driver circuits 1 and 2 work well at 10 MHz and higher and that they have similar rise time, fall time, and delay time: The rise time is about 3 ns, fall time is nearly 3 ns, and delay time is around 5 ns. Corner simulations have also been done to make sure that the circuit can work well at worst cases.

V. Layout and Design Considerations for the Driver IC Chip

A dedicated layout design has been required for ensuring the success and the reliability of the IC chip.

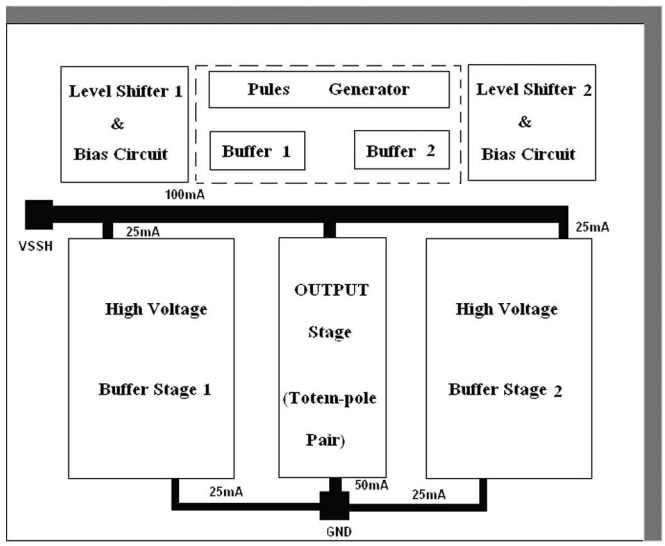


Fig. 7. Layout floorplan.

Fig. 7 shows the die floorplan for the driver, which sketches the locations and shapes of the individual cells.

Different aspects, including device matching, electrostatic discharge, electromigration, etc., need to be taken into account carefully during the layout design.

Three main considerations are reported hereafter.

A. Placements of the Cells

According to Fig. 7, the individual cells are represented by rectangles with the appropriate shapes and areas.

The design benefits from the use of mirror-image placements for the cells. This procedure ensures a good matching between

the bias circuits and the output HV voltage buffers and, consequently, similar electrical characteristics [24], [25].

B. Routing of the High-Current Leads

The large amount of output current, 50 mA, required to drive the GaN HFET devices at 10 MHz forces the use of layout techniques peculiar to high-current circuits. In particular, the routing of the high-current leads represents an important aspect for the reliability of the circuit.

Normally, electromigration sets a lower limit on the width of a high-current lead, but metal resistance often forces the use of much wider leads. In the design, all high-current leads have been kept as short as possible to minimize unnecessary metal resistance [25]. Fig. 7 shows the locations of the high-current leads along with the equivalent dc current they need to conduct.

The proposed locations of the high-current power leads $VSSH$ and GND make sure that these two leads can access all the related cells easily and with short lengths.

C. Layout Considerations of the LV Digital Circuit

As shown in Fig. 7, the digital circuit includes the pulse generator and two buffers in the doted block. The digital block is powered by the LV power supply, VDD. In order to obtain good isolation between the digital and the analog part of the circuit, we can benefit from the use of the integration process H35B4: This allows using floating LV devices instead of substrate-based LV devices for the LV digital circuit. This characteristic opens the design to several benefits [18].

1) Floating devices are more robust against substrate noise.
2) Substrate-based LV devices can generate substrate noise.
3) Substrate-based LV devices can collect substrate currents.
4) The area penalty for floating logic is negligible.
5) Substrate-based LV devices need additional layers (Standard NTUB and PTUB) for isolation.

D. Design of the Decoupling Capacitor

Since the target of the driver IC is to make GaN HFETs work at frequencies of 10 MHz and above, decoupling capacitor needs to be added in the IC layout in order to improve the power integrity and permit the circuit to work at high speed. In the circuit layout, decoupling capacitors were added as many as possible between the circuit blocks (such as between the pad ring and the core circuit).

VI. Test Results

The driver IC chip was fabricated as part of the multiproject die in the HV process H35B4 of Austriamicrosystems (which is available from MOSIS) in August 2008. The IC layout is shown in Fig. 8. Shown as the layout photograph, capacitors were added as many as possible in the spare space between the pad ring and the core circuit to act as decoupled transistor. The die size is 1745 μm $*$ 1640 μm. A 40DIP package was chosen for the chips by compromising the convenience for testing and

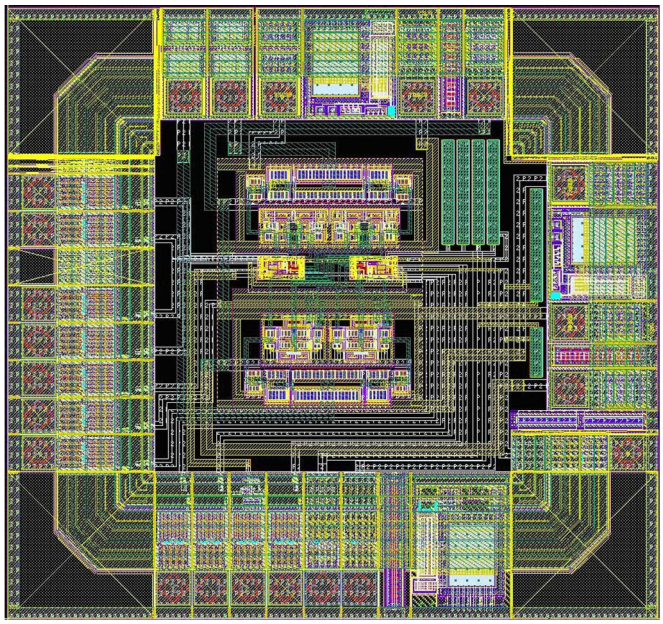


Fig. 8. Driver IC chip-top layout.

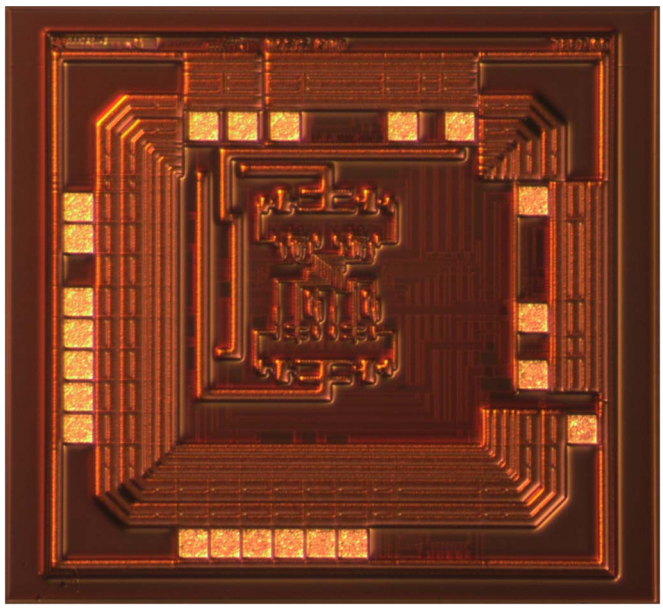


Fig. 9. Driver IC chip die photograph.

the values of the parasitic components. Fig. 9 shows the die photograph.

A prototype board was built to test the driver chip, and a series of experiments was made to verify the functionality and performance of the IC chip.

The schematic of the test circuit is shown in Fig. 10. In the test circuit, the GaN device is a 5-mm GaN HFET power device designed and fabricated at the semiconductor lab at the University of South Carolina. The experimental setup considered is the following: The control signals were generated by a high-speed FPGA board; a 100-Ω resistor, connected between the power supply $VDDH$ and the drain of the GaN HFET, acts as a load. The input capacitance for the GaN HFET is 20 pF. The resonant inductance in the circuit is 0.4 μH.

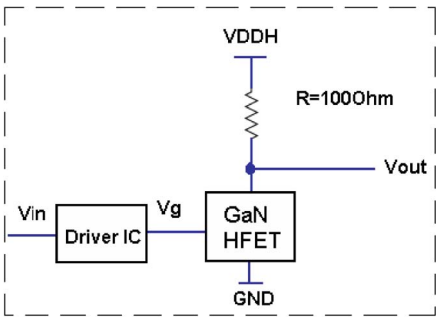


Fig. 10. Building block for the test circuit.

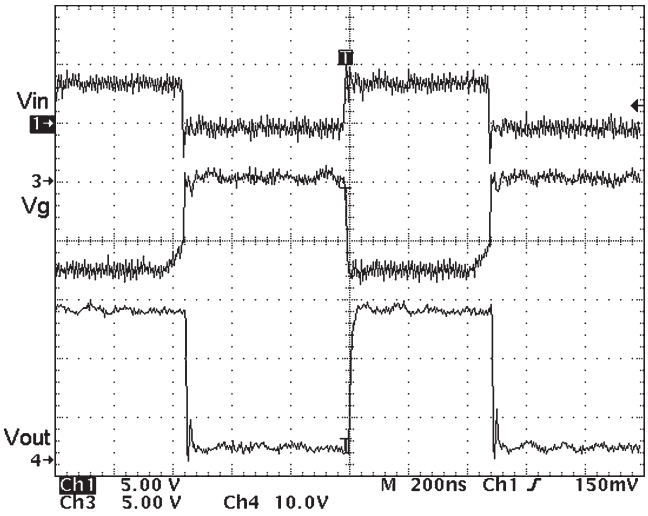


Fig. 11. Experimental measurements at 1 MHz.

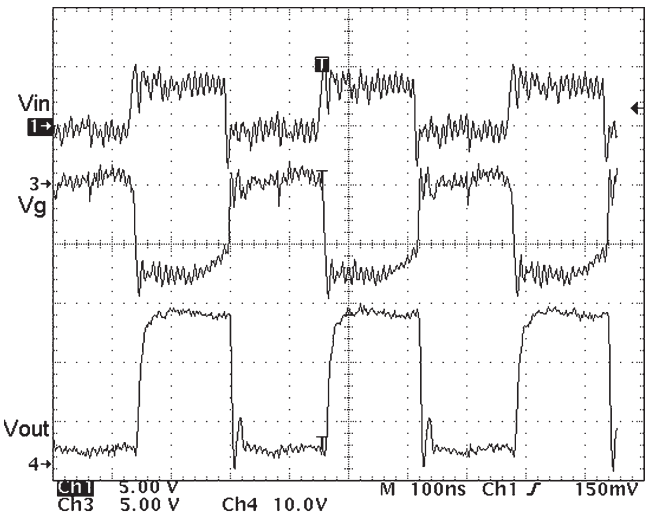


Fig. 12. Experimental measurements at 3.13 MHz.

During the tests, a series of $VDDH$ voltage increasing from 10 V is applied. In Figs. 11–14, $VDDH = 25$ V, and several switching frequencies, as shown in the photographs, have been considered.

The performances of both drivers in the driver chip were tested and verified. There are no big differences between the test waveforms for the two different driver circuits. In this paper, only the test waveforms of Driver 1 were shown. In

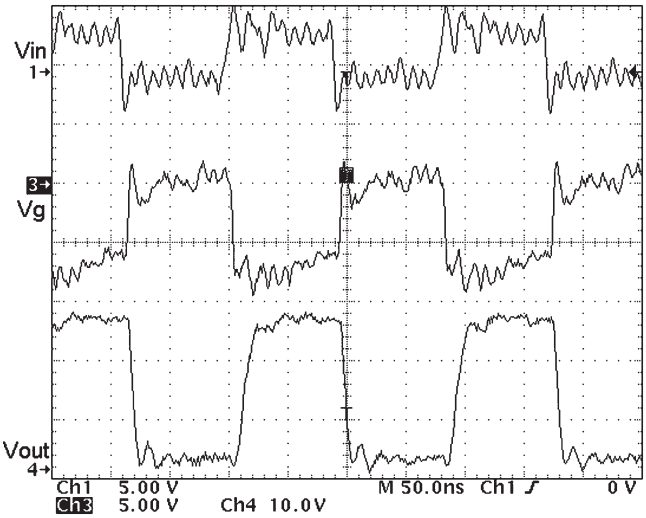


Fig. 13. Experimental measurements at 5 MHz.

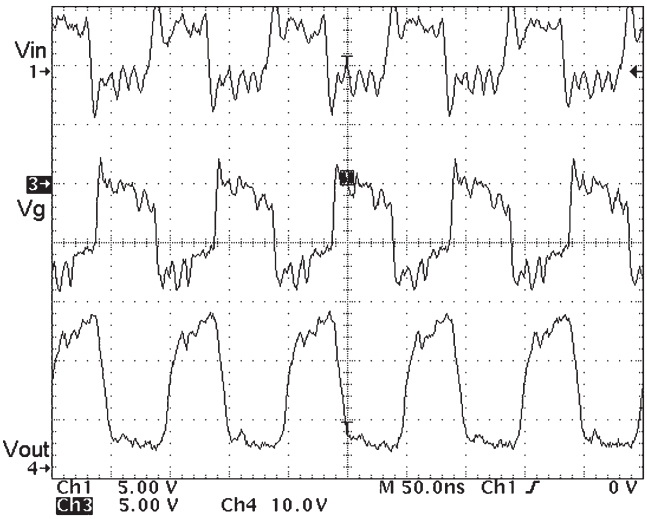


Fig. 14. Experimental measurements at 10 MHz.

Figs. 11–15, Channel 1 $V_{\rm in}$ is the control signal from the FPGA board, Channel 3 V_g is the gate drive signal from the driver IC, and Channel 4 $V_{\rm out}$ is the output signal at the drain of the GaN HFET. As confirmed by the tests, the drivers can command the switching of a GaN power device successfully at high frequencies (10 MHz).

Fig. 15 shows the transient waveforms at the device switching. The test results fully verified the performance of the driver IC and are similar to the simulation results shown in Fig. 6: The propagated delay for the driver IC is around 6 ns; the rise time and the fall time of the driver output signal are close to 4 ns.

VII. GaN-Based Boost Converter

A. Experimental Setup

A boost converter was built to further test the performances of the gate driver IC chip and to exploit the feasibility and advantages of GaN devices in power application.

Fig. 16 shows the schematic of the boost converter. In the boost converter circuit, a 5-mm GaN HFET with a total input

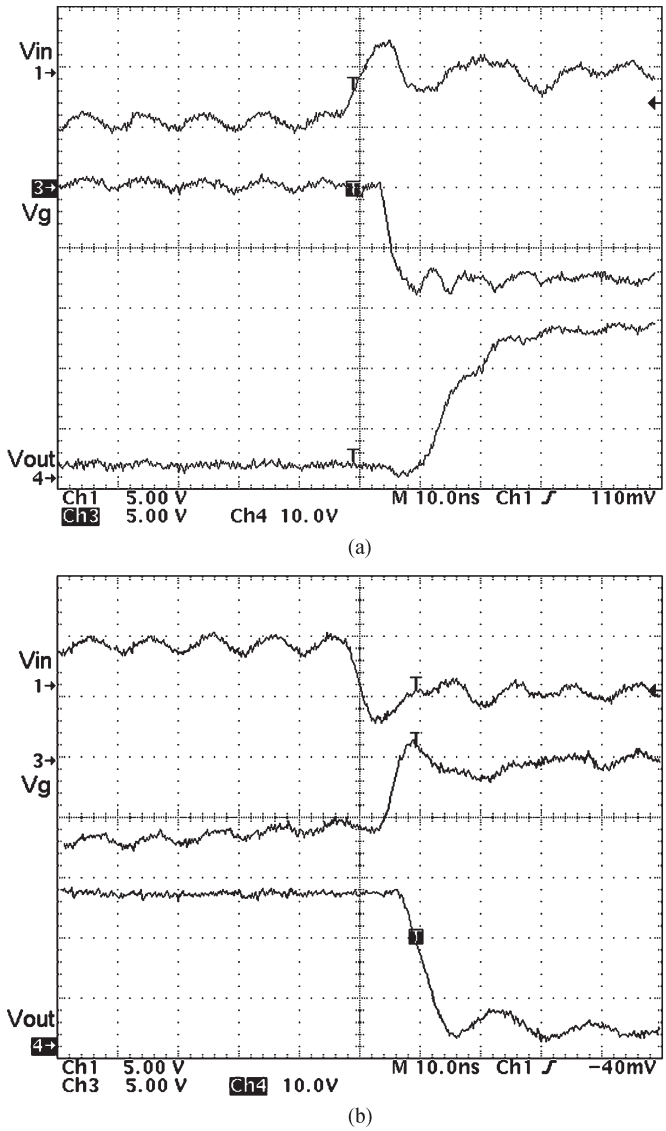


Fig. 15. Switching transient waveforms.

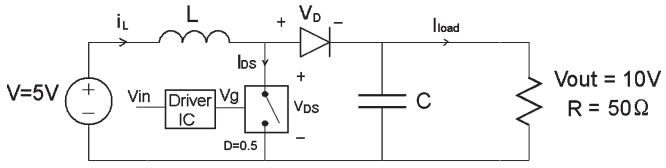


Fig. 16. Schematic of a boost converter.

capacitance of 20 pF and an on-resistance of 2 Ω was chosen as the power switch; the diode is a fast-speed Schottky diode MBR1060 with a forward voltage of 0.7 V; the input voltage V is 5 V; load resistor $R_{\rm load}$ is 50 Ω; and the output voltage $V_{\rm out}$ is 10 V. The duty cycle D and output current $I_{\rm load}$ can be calculated as

$$D = 1 - V/V_{\rm out} = 0.5 \tag{10}$$

$$I_{\rm out} = V_{\rm out}/R_{\rm load} = 10/50 = 0.2\ \text{A}. \tag{11}$$

Choosing 1/4 $I_{\rm out}$ as the inductor current ripple, 0.025 $V_{\rm out}$ as the output voltage ripple, and 1 MHz as the switching frequency, we can calculate the values of the inductor and capacitor as follows:

$$L = \frac{V}{\Delta i_L} * \frac{D}{f_s} = \frac{5 * 0.5}{0.05 * 1 * 10^6} = 50\ \mu\text{H} \tag{12}$$

$$C = \frac{V_{\rm out}}{R * \Delta v_c} * \frac{D}{f_s} = \frac{10 * 0.5}{50 * 0.25 * 1 * 10^6} = 400\ \text{nF} \tag{13}$$

where

Δi_L inductor current ripple;
Δv_c output voltage ripple;
f_s switching frequency.

B. Test Results

Fig. 17 shows the test waveforms for the boost converter at switching frequencies of 1, 3.13, and 10 MHz. In Fig. 17, Channel 1 is the 3.3-V input control signal from FPGA, Channel 2 is the inductor current, Channel 3 is the driver IC output signal, and Channel 4 is the output voltage.

As shown in Fig. 17, the boost converter works well; the output voltage and inductor current are at the same values as that we calculated. When we increase the switching frequency, the inductor current ripple decreases, or smaller inductor and capacitor can be used to obtain the same inductor current ripple and output voltage ripple. However, the increasing frequency also leads to increased switching power loss and, hence, decreased circuit efficiency.

C. Power Loss Calculation

Fig. 18 shows the drain current and drain–source voltage for the GaN device in the boost converter at the turn-off switching; the turn-on waveform is similar. The drain current is around 0.2 A, the drain–source voltage is around 10 V, the crossover time between the drain–source voltage and drain current is around 13 ns. The switching energy can be calculated as

$$\begin{aligned} E_{\rm sw} &= E_{\rm on} + E_{\rm off} = 1/2 * V_{\rm DS} * I_{\rm DS} * (t_r + t_f) \\ &= 0.5 * 10 * 0.2 * (13 + 13) * 10^{-9} = 26 * 10^{-9}\ \text{J} \end{aligned} \tag{14}$$

where

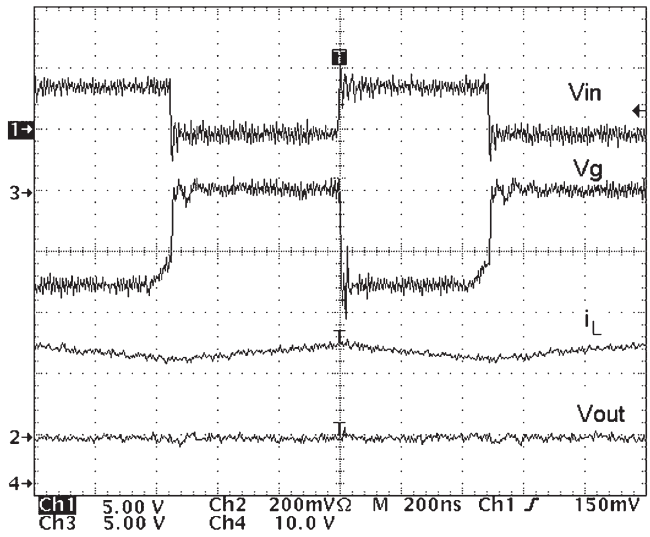
$E_{\rm sw}$ switching energy;
$E_{\rm on}$ switching energy at device turn-on;
$E_{\rm off}$ switching energy at device turn-off;
$V_{\rm DS}$ drain–source voltage of the GaN device;
$I_{\rm DS}$ drain current of the GaN device;
t_r and t_f rise time and fall time.

Given that the series gate resistance of the GaN device is 0.1 Ω, the input capacitance is 20 pF, and the resonant inductance is 0.4 μH, the gate energy can be calculated as[4]

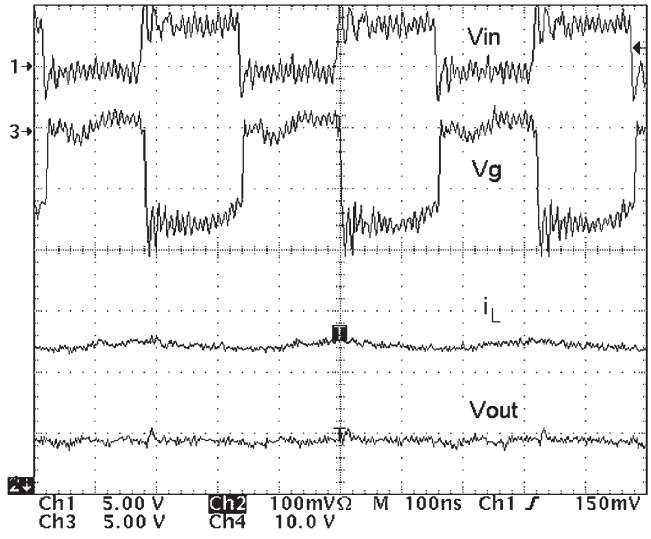
$$\begin{aligned} E_g &= \frac{\pi}{2} \frac{R_G}{\sqrt{L_R/C_{\rm iss}}} C_{\rm iss} V_g^2 \\ &= \frac{3.14 * 0.1 * 20 * 10^{-12} * 7^2}{2 * \sqrt{0.4 * 10^{-6}/20 * 10^{-12}}} = 1.25 * 10^{-12}\ \text{J} \end{aligned} \tag{15}$$

where

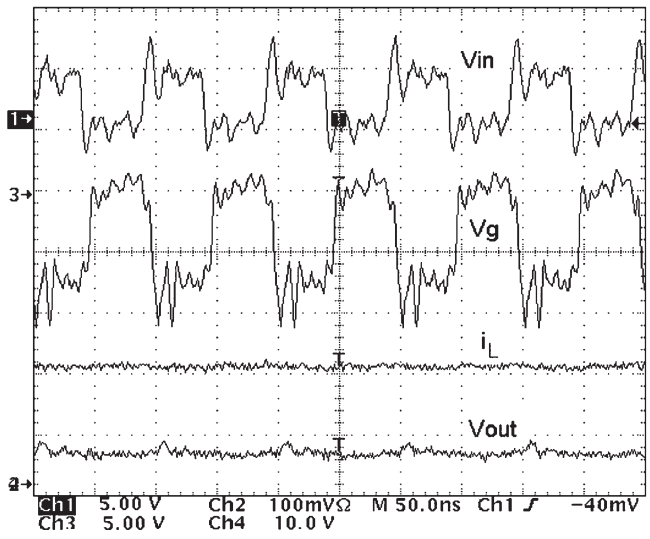
E_g gate energy of the GaN device;
R_G series gate resistance of the GaN device;



(a)



(b)



(c)

Fig. 17. Test waveform. (a) 1 MHz. (b) 3.13 MHz. (c) 10 MHz.

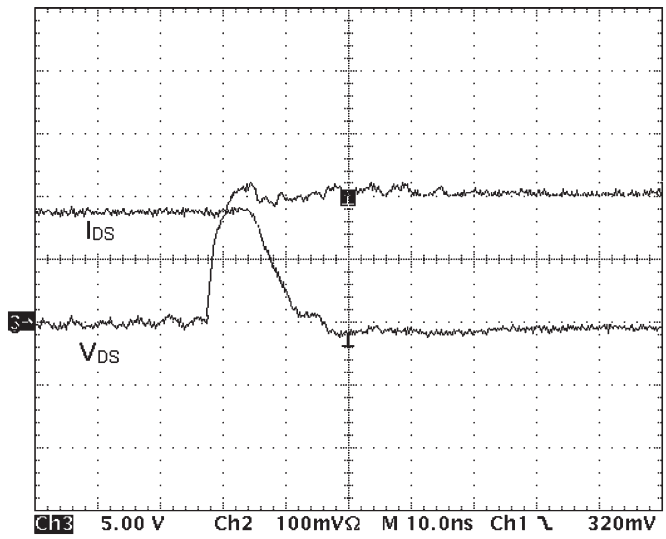


Fig. 18. Turn-off transient waveform.

L_R resonant inductance in the drive circuit;
$C_{\rm iss}$ input capacitance of the GaN device.

Given that the on-resistance of GaN HFET is 2 Ω and the forward voltage of the diode is 0.7 V, the conduction loss in the circuit consists of the conduction loss of the GaN HFET and of the diode and can be calculated as follows:

$$\begin{aligned} P_{\rm cond} &= P_{\rm HFET} + P_D \\ &= R_{\rm ON} * I_{\rm DS}^2 * D + V_D * I_{load} * (1 - D) \\ &= 2 * 0.2^2 * 0.5 + 0.7 * 0.2 * 0.5 = 0.11 \text{ W} \end{aligned} \quad (16)$$

where

$P_{\rm cond}$ conduction power loss;
$R_{\rm ON}$ on-resistance of the GaN device;
V_D forward voltage of the diode.

Integrating (14)–(16) together, the total power loss in the boost converter can be obtained at a switching frequency of 1 MHz

$$\begin{aligned} P_{\rm loss} &= P_{\rm cond} + (E_{\rm sw} + E_g) * f_s \\ &= 0.11 + (26 * 10^{-9} + 1.25 * 10^{-12}) * 1 * 10^6 \\ &= 0.136 \text{ W}. \end{aligned} \quad (17)$$

It is clear that the conduction loss is dominant in this boost converter circuit at a switching frequency of 1 MHz. Increasing the switching frequency will lead to an increase of the total power loss in the circuit. At 10 MHz, the switching power loss dominates the total power loss in the converter. At this situation, a smaller resonant inductor needs to be used to speed up the turn-on and turn-off of the GaN device in order to decrease the switching power loss.

VIII. Summary and Future Work

In this paper, the IC implementation of the diver circuit introduced in [4] and [14] for 100-V 1-A GaN HFET switching at 10 MHz has been described.

The layout design and the implementation process are discussed, underlining the different options settled.

The test results shown fully confirm the possibility to exploit the peculiar characteristics of GaN devices in power electronics.

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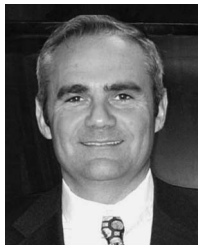

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