DPUs on the FABRIC Testbed

Elie Kfoury*, Jennifer Kim^, Jorge Crichigno*
* College of Engineering and Computing, University of South Carolina
^ Internet2

Internet2 Technology Exchange (TechEx)

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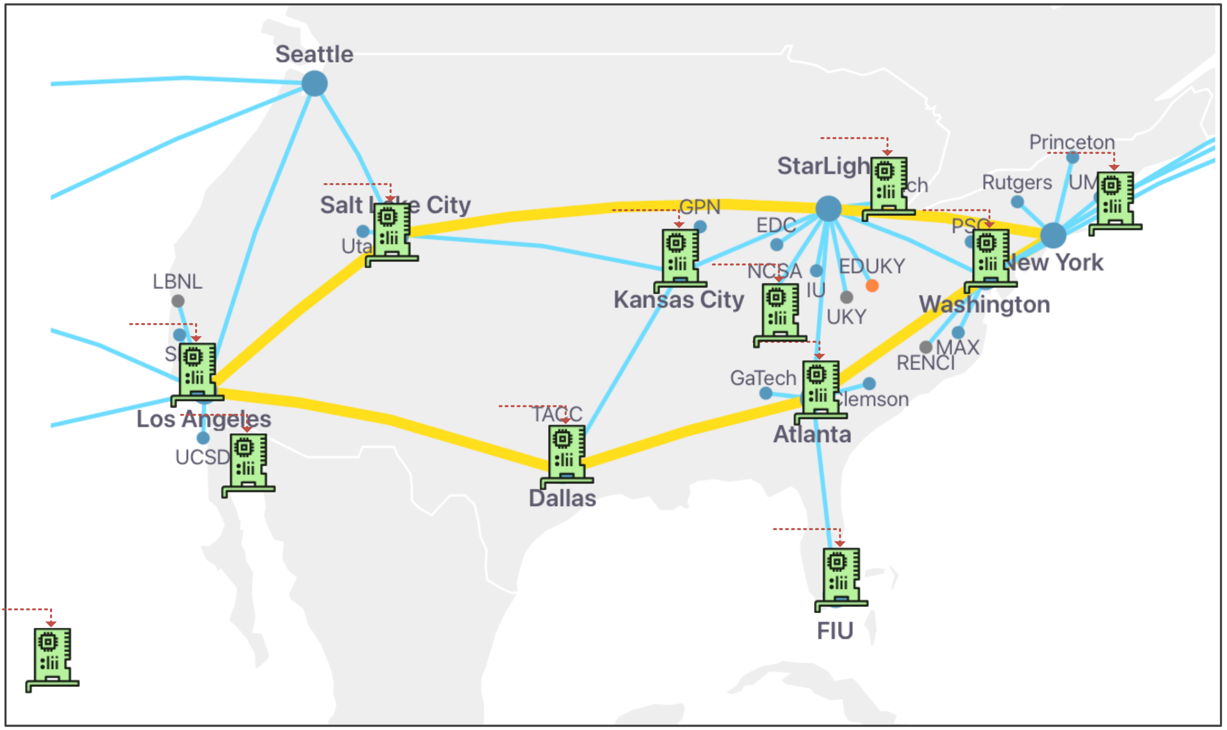
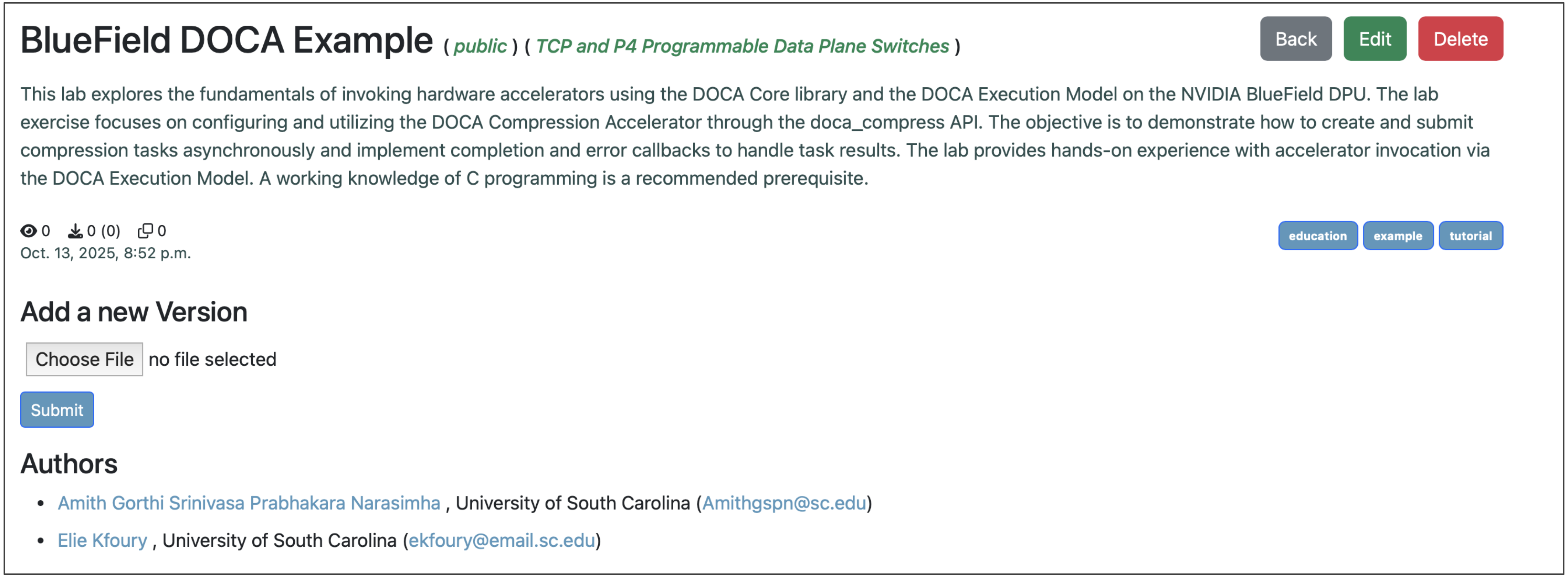
DPUs on FABRIC

- BlueField-3 DPUs are installed on various FABRIC sites
- Currently the following sites have DPUs installed (more will be available soon):
  - 100G DPU: TACC, MICH, MASS, NCSA, DALL, FIU, LOSA, KANS, NEWY, ATLA, SEAT, PSC, RUTG, HAWI
  - 400G DPU: SALT, WASH



DOCA Example on Artifact Manager

- Compression acceleration example is available on the Artifact Manager



BlueField DOCA Example (*public*) (*TCP and P4 Programmable Data Plane Switches*)

This lab explores the fundamentals of invoking hardware accelerators using the DOCA Core library and the DOCA Execution Model on the NVIDIA BlueField DPU. The lab exercise focuses on configuring and utilizing the DOCA Compression Accelerator through the doca_compress API. The objective is to demonstrate how to create and submit compression tasks asynchronously and implement completion and error callbacks to handle task results. The lab provides hands-on experience with accelerator invocation via the DOCA Execution Model. A working knowledge of C programming is a recommended prerequisite.

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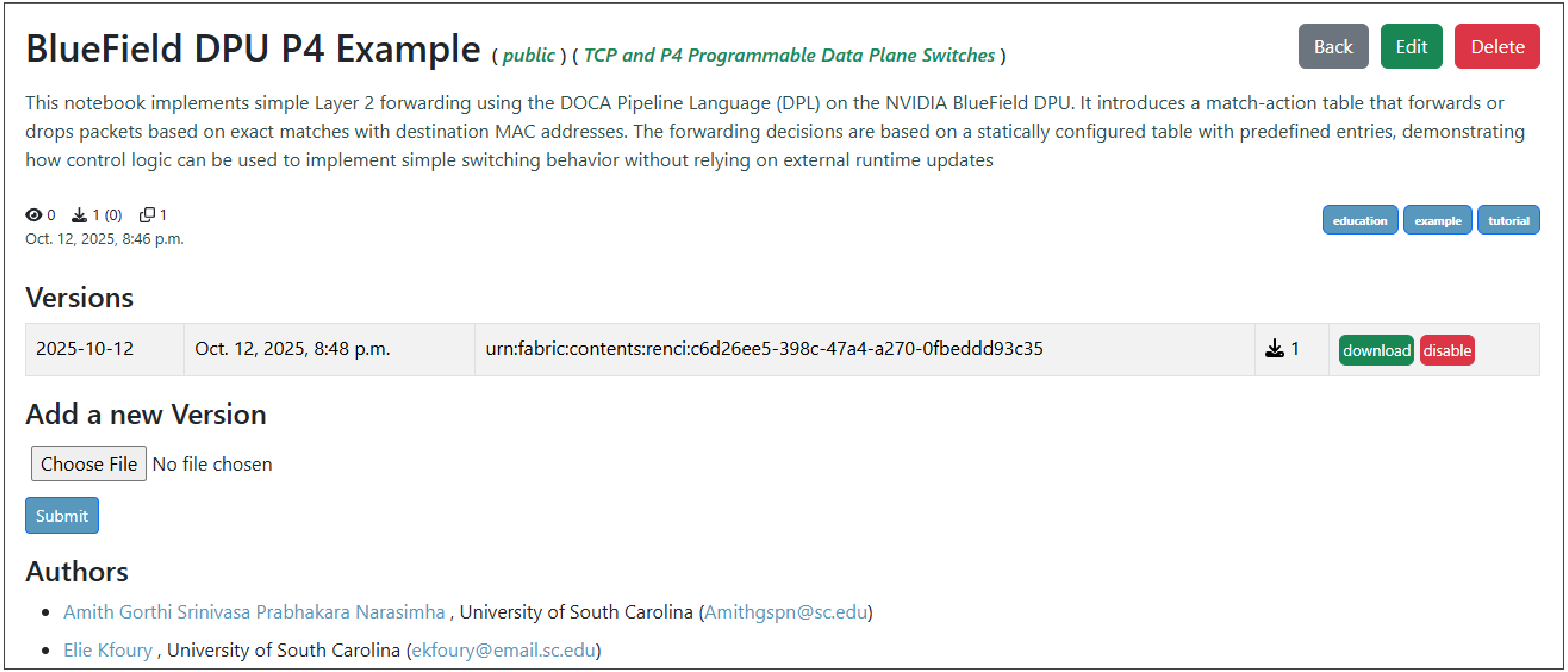
Authors

- Amith Gorthi Srinivasa Prabhakara Narasimha , University of South Carolina (Amithgspn@sc.edu)
- Elie Kfoury , University of South Carolina (ekfoury@email.sc.edu)

P4 Example on Artifact Manager

- Simple L2 forwarding example available on Artifact Manager



BlueField DPU P4 Example *(public) (TCP and P4 Programmable Data Plane Switches)*

This notebook implements simple Layer 2 forwarding using the DOCA Pipeline Language (DPL) on the NVIDIA BlueField DPU. It introduces a match-action table that forwards or drops packets based on exact matches with destination MAC addresses. The forwarding decisions are based on a statically configured table with predefined entries, demonstrating how control logic can be used to implement simple switching behavior without relying on external runtime updates

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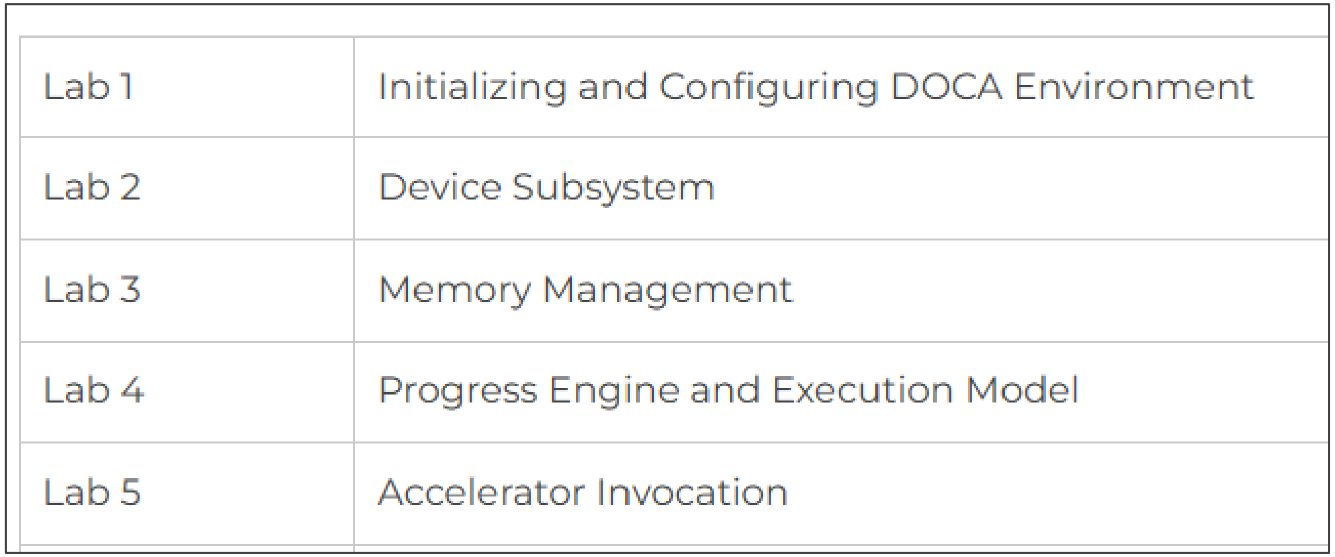
DPU Labs

- DPU cybertraining is supported by NSF Cybertraining program, award #2417823
- Lab libraries available to learn about DPU programming:
  - **DPU Programming using DOCA**
  - DPU Programming using P4 DPL
  - Introduction to P4-DPDK
  - P4-DPDK Security applications



Lab 1	Initializing and Configuring DOCA Environment
Lab 2	Device Subsystem
Lab 3	Memory Management
Lab 4	Progress Engine and Execution Model
Lab 5	Accelerator Invocation

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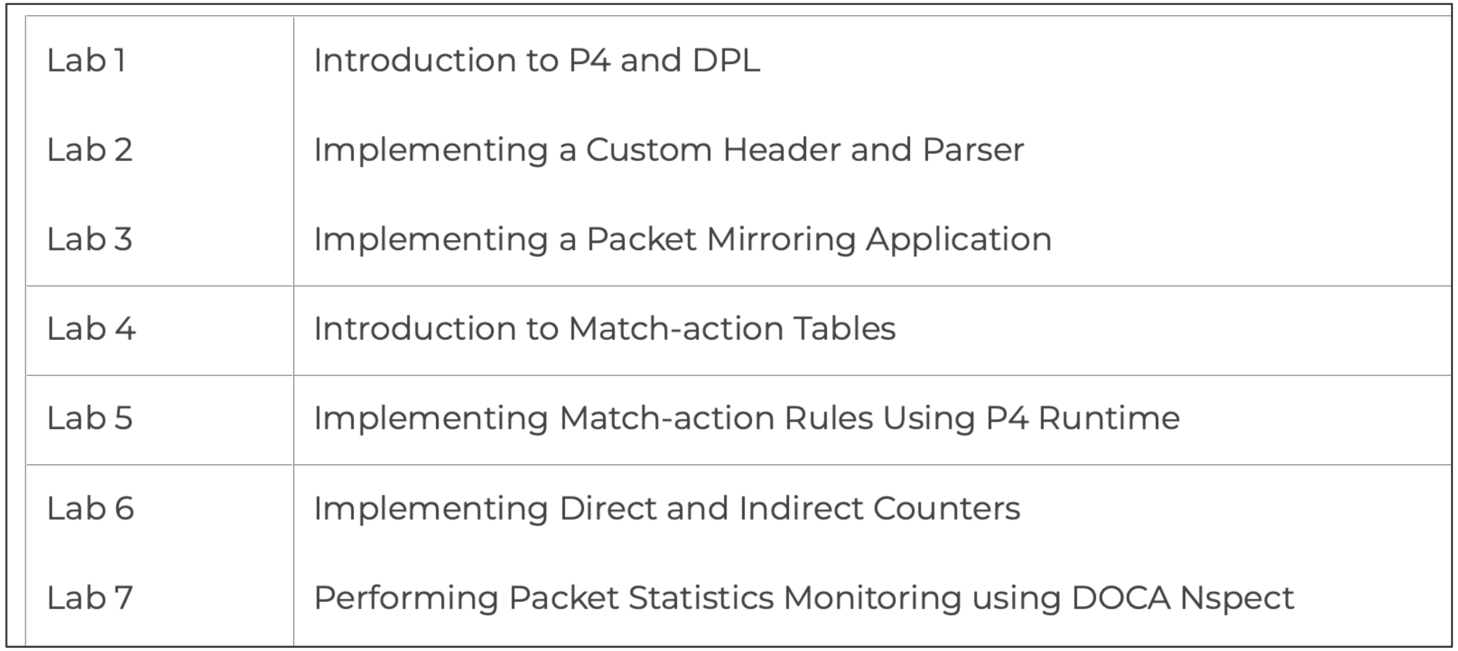

Lab 1	Introduction to P4 and DPL
Lab 2	Implementing a Custom Header and Parser
Lab 3	Implementing a Packet Mirroring Application
Lab 4	Introduction to Match-action Tables
Lab 5	Implementing Match-action Rules Using P4 Runtime
Lab 6	Implementing Direct and Indirect Counters
Lab 7	Performing Packet Statistics Monitoring using DOCA Nspect

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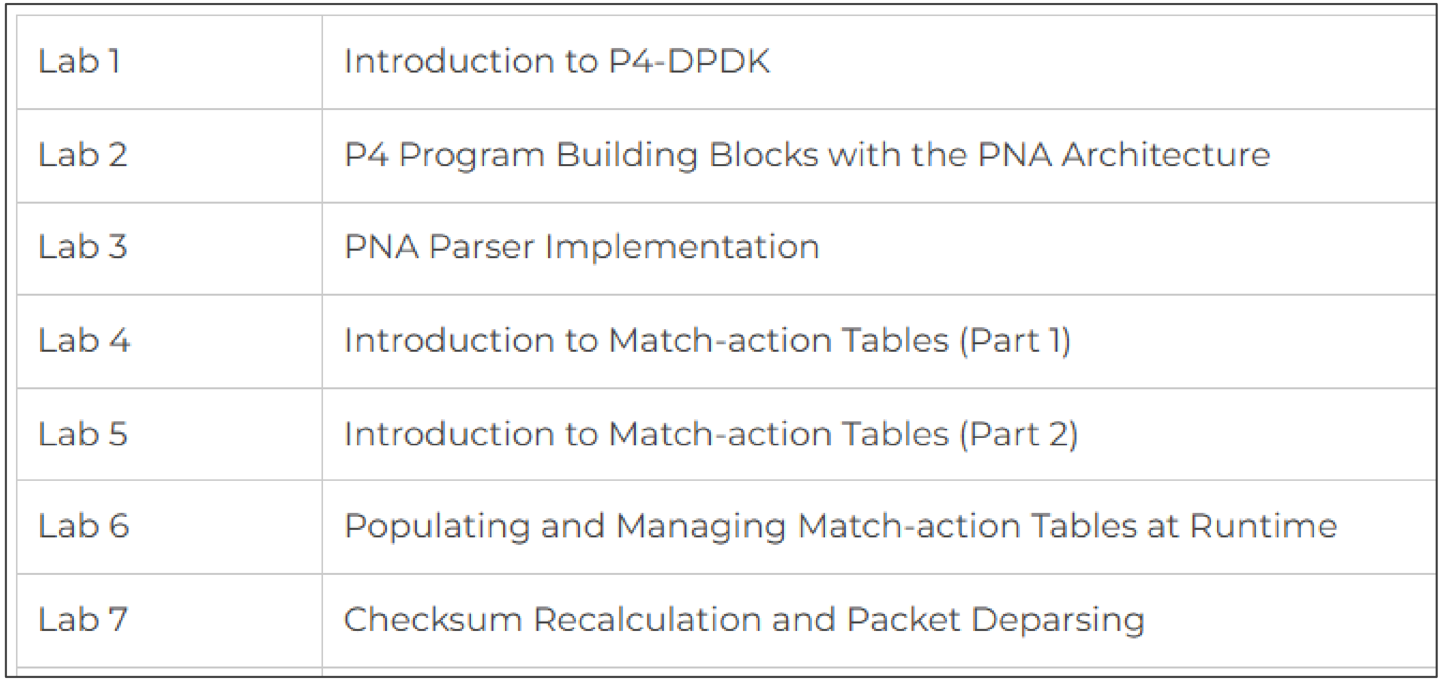

Lab 1	Introduction to P4-DPDK
Lab 2	P4 Program Building Blocks with the PNA Architecture
Lab 3	PNA Parser Implementation
Lab 4	Introduction to Match-action Tables (Part 1)
Lab 5	Introduction to Match-action Tables (Part 2)
Lab 6	Populating and Managing Match-action Tables at Runtime
Lab 7	Checksum Recalculation and Packet Deparsing

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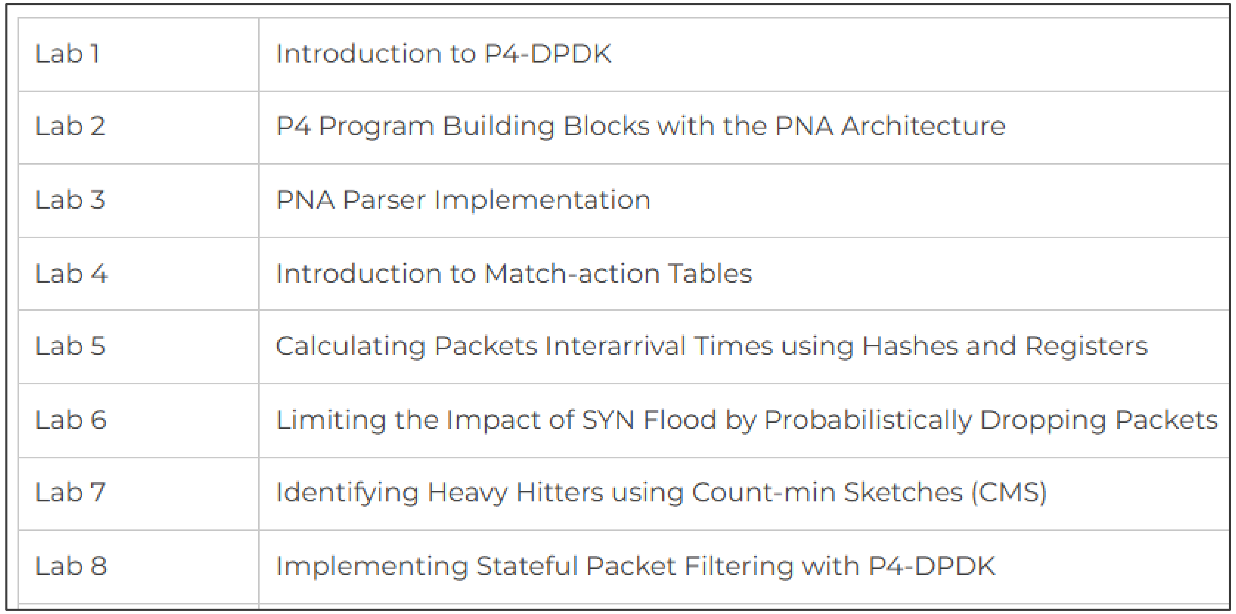
  - Introduction to P4-DPDK
  - **P4-DPDK Security applications**



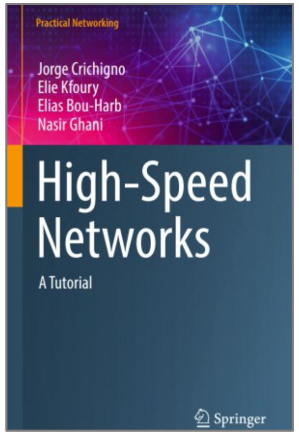
Lab 1	Introduction to P4-DPDK
Lab 2	P4 Program Building Blocks with the PNA Architecture
Lab 3	PNA Parser Implementation
Lab 4	Introduction to Match-action Tables
Lab 5	Calculating Packets Interarrival Times using Hashes and Registers
Lab 6	Limiting the Impact of SYN Flood by Probabilistically Dropping Packets
Lab 7	Identifying Heavy Hitters using Count-min Sketches (CMS)
Lab 8	Implementing Stateful Packet Filtering with P4-DPDK

Cybertraining Material Developed at USC

Information about lab libraries is available at: https://research.cec.sc.edu/cyberinfra/cybertraining

Programmable data plane devices

1. DPU Programming using P4
2. DPU Programming using DOCA
3. P4-DPDK Security
4. Introduction to P4-DPDK
5. Cybersecurity Apps with P4 Programmable Data Planes
6. P4 Programmable Data Planes: Applications, Stateful Elements, Custom Packet Processing
7. Intro to P4 Programmable Switches
8. Intro to P4 Programmable Switches with Intel’s Tofino
9. P4 Monitoring Applications



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Acknowledgement

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