Introductory and Advanced Topics on P4 Programmable Data Plane Switches

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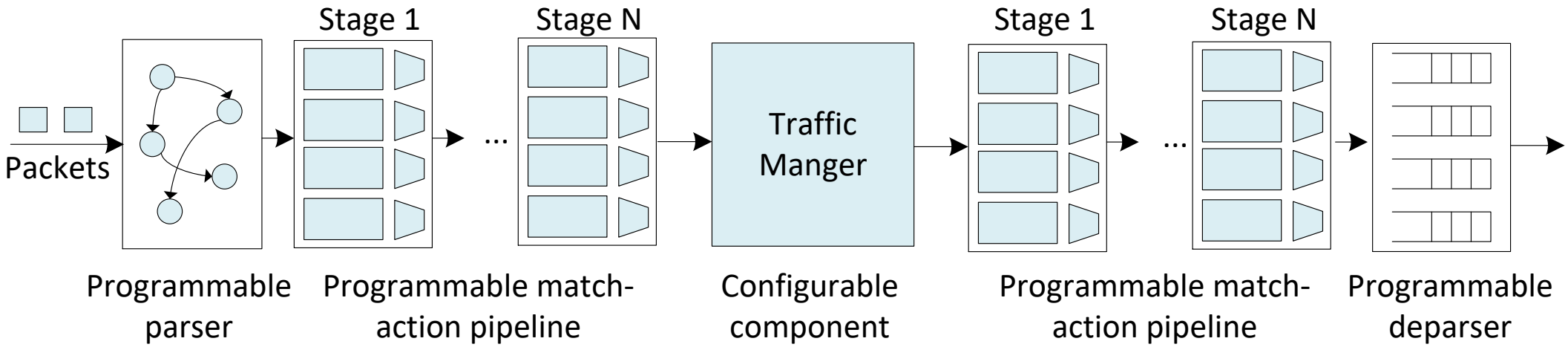
P4 Program Building Blocks

Lab activities are described in Lab 3, P4 Programmable Data Plane Switches (BMv2) lab series

V1Model

- Common $P4_{16}$ architecture used with BMv2
- Implemented on top of BMv2's *simple_switch* target
- It consists of a programmable parser, an ingress match action pipeline, a traffic manager, an egress match-action pipeline, and a deparser



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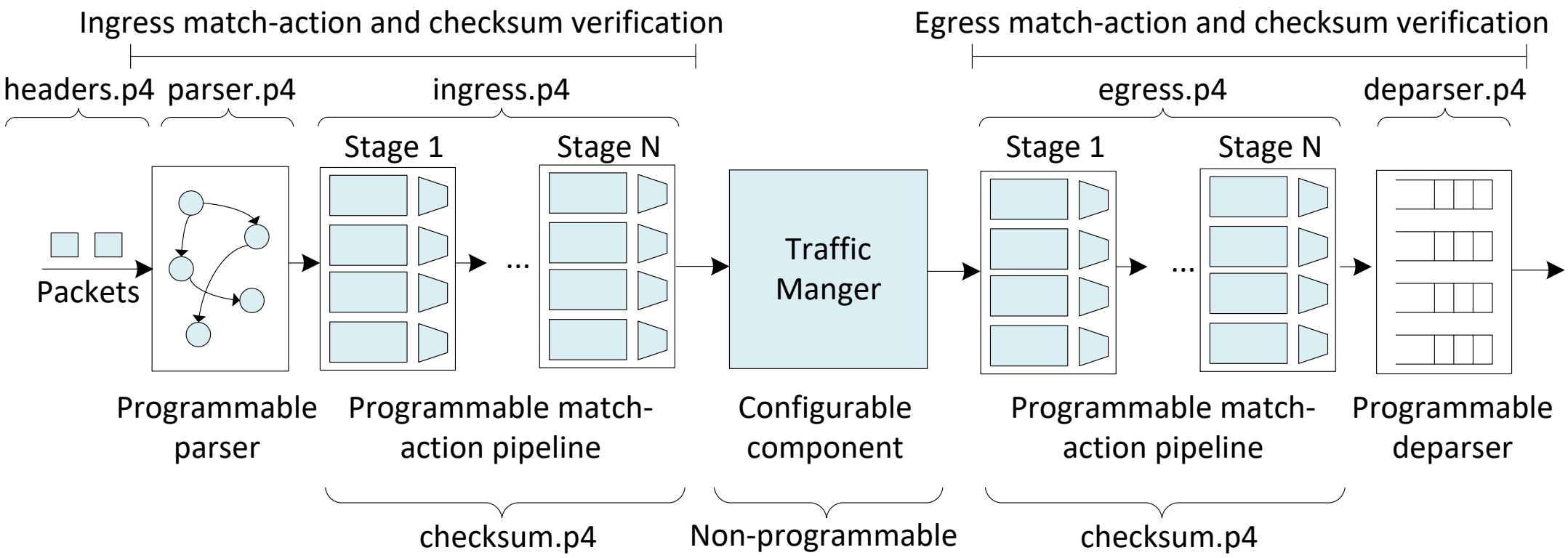

Lab Topology and Objectives

- The topology consists of two hosts: h1 and h2; one P4 switch: s1
- Mapping the P4 program components to the components of the programmable pipeline
- Trace the lifecycle of a packet as it traverses the pipeline